LOW FREQUENCY NOISE IN HYDROGENATED AMORPHOUS SILICON THIN FILM TRANSISTORS

A Thesis Submitted to the College of

Graduate Studies and Research

in Partial Fulfillment of the Requirements

for the Degree of Master of Science

in the Department of Electrical Engineering

University of Saskatchewan

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Keywords: low frequency noise, amorphous silicon, thin-film transistor

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ABSTRACT

Hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) are used as charge switches in flat-panel X-ray detectors. The inherent noise in the TFTs contributes to the overall noise figure of the detectors and degrades the image quality. Measurements of the noise provide an important parameter for modeling the performance of the detectors and are a sensitive diagnostic tool for device quality. Furthermore, understanding the origins of the noise could lead to change a method of a-Si:H deposition resulting in a reduction of the noise level. This thesis contains measurements of the low-frequency noise in a-Si:H TFTs with an inverted staggered structure. The noise power density spectrum fits well to a $1/f^{\alpha}$ power law with α near one. The normalized noise power is inversely proportional to gate voltage and also inversely proportional to channel length in both the linear and saturation regions. The noise is nearly independent of the drain-source voltage and drain-source current. The noise is unaffected by degrading the amorphous silicon through gate-biasing stress. Hooge's parameter is in the range $1\text{-}2\times10^{-3}$ or $2\text{-}4\times10^{-4}$ depending on whether the parameter is calculated using the total number of charge carriers in the accumulation layer or just the number of free carriers. As an example, the signal to noise ratio is calculated for photodiode detector gated by a TFT using the results from the noise measurements.

ACKNOWLEDGMENTS

First, I would like to express my sincere gratitude to my supervisor, Dr. Robert Johanson, and co-supervisor, Dr. Safa O. Kasap, for giving me the opportunity to study in the field and providing financial support and advice. I would like to thank the Nanoelectronics Research Group, the University of Waterloo, for providing the a-Si:TFT samples; especially, Dr. Peyman Servati for providing me with advice. I would like to thank all members of my research group; especially, George Belev, Hasib Majid, Zahid Shakoor, and Yang Xu, for their friendship and assistance. Finally, I would like to thank my parents and my family, Ejin and Jungmin, for their patience and love.

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LIST OF ABBREVIATIONS

a-Si:H	Hydrogenated amorphous silicon
B_2H_6	Diborane
B	The bandwidth of the measurement
BCE a-Si:H TFT	The back-channel-etched a-Si:H TFT
C	Capacitor
C_{ins}	Insulator capacitance
C_g	The capacitance of the gate dielectric
DOS	The density of states
d	Thickness of channel
E_F	Fermi energy
ES a-Si:H TFT	Etch-stopper a-Si:H TFT
FFT	Fourier Fast Transform
FET	Field Effect Transistor
G_1 and G_2	Gains of amplifiers
HEMT	High electron mobility transistor
HIGFET	Hetero-structure insulated gate field effect transistor
IGFET	Insulated gate field effect transistor
I_d	dc current
I_{ds}	Drain-source current
JFET	Junction Field Effect Transistor
K	Integrated noise power
k	Boltmann's constant (1.38×10^{-23} J/°K)
LW	Frequency line width
L:W aspect ratio	Ratio of channel length to width
L	Channel length
LCD	Liquid Crystal Display
MESFET	Metal-Semiconductor FET
MOSFET	Metal-oxide-semiconductor field-effect transistor
NH_3	Ammonia gas
N_2	Nitrogen gas
n	The density of carriers
PH_3	Phosphine
q	Electronic charge

R	Resistor
R	Resistance
RMS	The root-mean-square
SiH_4	Silane gas
SOS MOSFET	Silicon-on-saphire MOSFET
SIT	Static induction transistor.
S_n	Normalized current noise power density
S_I	Current noise power density
S_V	Voltage noise power density
S_R	Resistance noise power density
S_G	Conductance noise power density
S_μ	Mobility noise power density
SNR	Signal-to-noise ratio
t_{ins}	Thickness of the insulator
t_{ox}	The thickness of a gate dielectric
t	Time
TFT	Thin-film field effect transistor
T	Absolute temperature
V_T	Threshold voltage
V_d	Drain Voltage
V_g	Gate Voltage
V_p	Pinchoff Voltage
V_{ds}	Drain-source voltage
w	Depletion width
W	Channel width
α_H	Hooge's parameter
ε_R	Relative permittivity
ε_{ins}	Permittivity of the insulator
μ	Mobility
σ	Conductivity

1. INTRODUCTION

The thesis work involves measurements of thin-film field effect transistors (TFTs), specifically TFTs made from hydrogenated amorphous silicon (a-Si:H). This chapter presents the fundamentals of field effect transistors (FETs) and their categorization. In addition, one of the applications of a-Si:H TFTs is surveyed. In the last part, the objectives of the research are introduced.

1.1 Field Effect Transistors

One of the most important types of semiconductor devices is the field effect transistor (FET). The device operates as a capacitor with one plate that serves as a conducting channel between two ohmic contacts, the source and the drain. The other plate, the gate, controls the charge induced into the channel. The carriers in the channel come from the source and move across the channel into the drain. This basic principle has been exploited in a variety of different types of FETs as shown Fig. 1.1. These devices are distinguished by the gate material, by how the gate is isolated from the channel, and by what type of carrier is induced by the gate voltage into the channel (electrons in n-channel devices, holes in p-channel devices). The FETs can be roughly classified into two groups depending on whether or not they have an insulator that prevents conduction between the gate electrode and the channel, insulated gate field effect transistors (IGFETs), or not, junction field effect transistors (JFETs). JFETs are fabricated on bulk substrates and include silicon JFETs and static induction transistors (SITs) that show both

bipolar and field effect phenomena. GaAs MESFETs (Metal-Semiconductor FETs) fabricated in an epitaxial or implanted layer on a semi-insulating substrate are another example of a JFET.

The IGFETs are classified into two groups depending on how they are fabricated: metal-oxide-semiconductor field-effect transistors (MOSFETs) and thin-film transistors (TFTs). MOSFETs are fabricated on a bulk silicon wafer, while TFTs are made from a thin-film semiconductor layer deposited on a glass substrate, such as a-Si:H. The most common MOSFETs are those constructed on silicon wafers which use silicon dioxide for the gate insulator, and currently these form the foundation of the modern electronics industry. High electron mobility transistors (HEMT) made from GaAs, and hetero-structure insulated gate field transistors (HIGFET) are other examples of MOSFET and are also fabricated on bulk substrates. The TFTs include thin-film field effect transistors and silicon-on-saphire (SOS) MOSFETs [1].

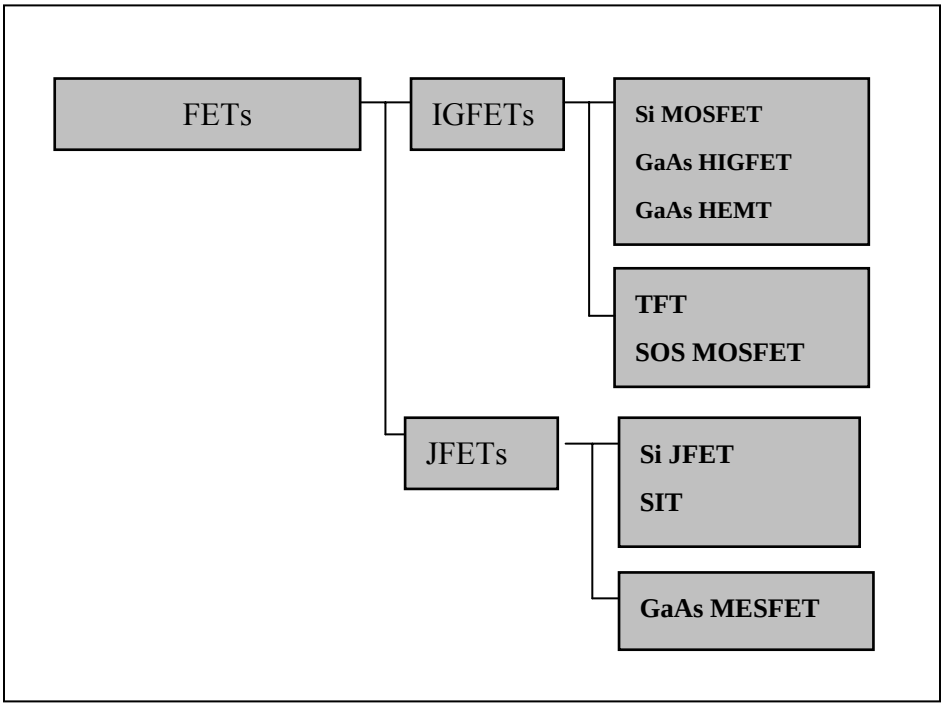


Figure 1.1 A classification of field effect transistors [1].

The basic operation of a typical MOSFET is shown in Fig. 1.2a-c where t_i is the thickness of gate insulator. If the semiconductor is naturally p-type and a negative gate voltage is applied, additional holes accumulate at the semiconductor-insulator interface. Conversely, if a positive gate voltage is applied, the holes are repelled from the interface and the underlying semiconductor layer becomes depleted or, if the gate voltage is large enough (beyond the threshold voltage), electrons will accumulate and the layer becomes inverted. The depletion width (w) increases with increasing gate voltage until the threshold voltage (V_T) is reached. Above V_T, almost all the additional charge goes toward increasing the electrons in the narrow inversion layer and the depletion width remains virtually constant at W_T. The conductivity of the channel changes depending on the carrier concentration in the channel which is controlled by the gate voltage. The conductivity is the product of the charge (q), the density of carriers (n) and the carrier mobility (μ), $\sigma = qn\mu$. When the channel is depleted, the free-carrier concentration is greatly reduced and the source-drain conductance decreases. On the other hand, when the channel is inverted, a highly conducting channel of the opposite carrier type to

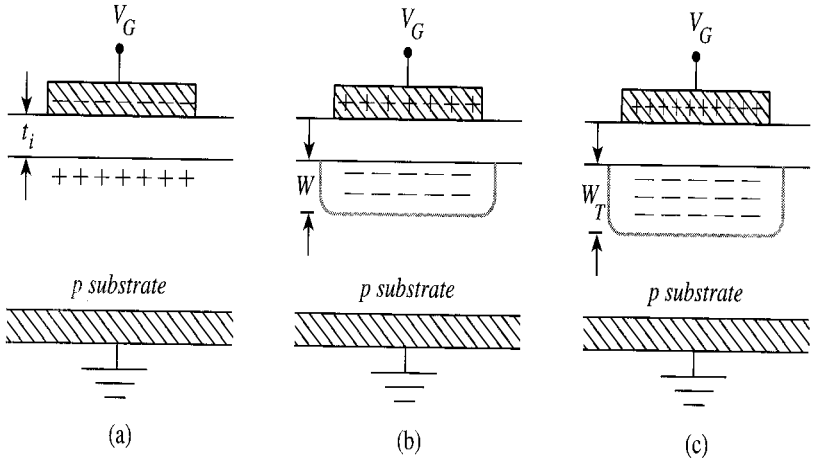


Figure 1.2 The MOS capacitor for various bias conditions. (a) accumulation (Vg < 0)); (b) depletion (V_T > Vg > 0); and (c) at the threshold of strong inversion (V_T =Vg) [1].

that of the bulk semiconductor material forms at the semiconductor-insulator interface.

The current in the channel flows between more heavily doped regions, the source and the drain, which in this device would be doped n^+. Little current flows for negative gate voltages because, although the channel is conductive, the n^+p junctions form back to back diodes one of which is always reversed biased. For the same reason, the source-drain current will be small for positive gate voltages below V_T (Fig. 1.3a). Above the threshold, a source-drain voltage will cause a current to flow because the n^+ to inverted channel contact is ohmic (Fig. 1.3b and c). For a positive drain voltage (V_D) (source grounded), the density of electrons in the inversion layer decreases from the source side to the drain side because the voltage of the drain reduces the potential difference between the gate and the channel. When $V_D = V_G - V_T$, the inversion charge density reaches zero (pinchoff) at the drain (Fig. 1.3d). For larger V_D, the pinchoff point moves away from the drain but the voltage at the pinchoff point remains $V_P = V_G - V_T$ (Fig. 1.3e). The electron current in the channel is injected into the depletion region at the pinchoff point by the large electric field and flows on to the drain (Fig. 1.3e). The source-drain current is mainly determined by the potential drop across the inverted region. Below pinchoff, the drop is V_D, and so the current is linear with V_D. Above pinchoff, the drop is just V_P which is a constant for a given gate voltage, so the current is roughly independent of V_D. The above results in the typical I-V characteristics of an enhancement-mode MOSFET as shown in Fig. 1.3f [1].

An important use of an FET is a switch and it is this use that is central to this thesis. When used as a switch, the FET is either "on" or "off". When "on", the gate voltage is sufficient to produce a highly conducting channel between the source and the drain. Alternatively, when "off", that is zero gate voltage is applied, no channel exists and only a small leakage current can flow.

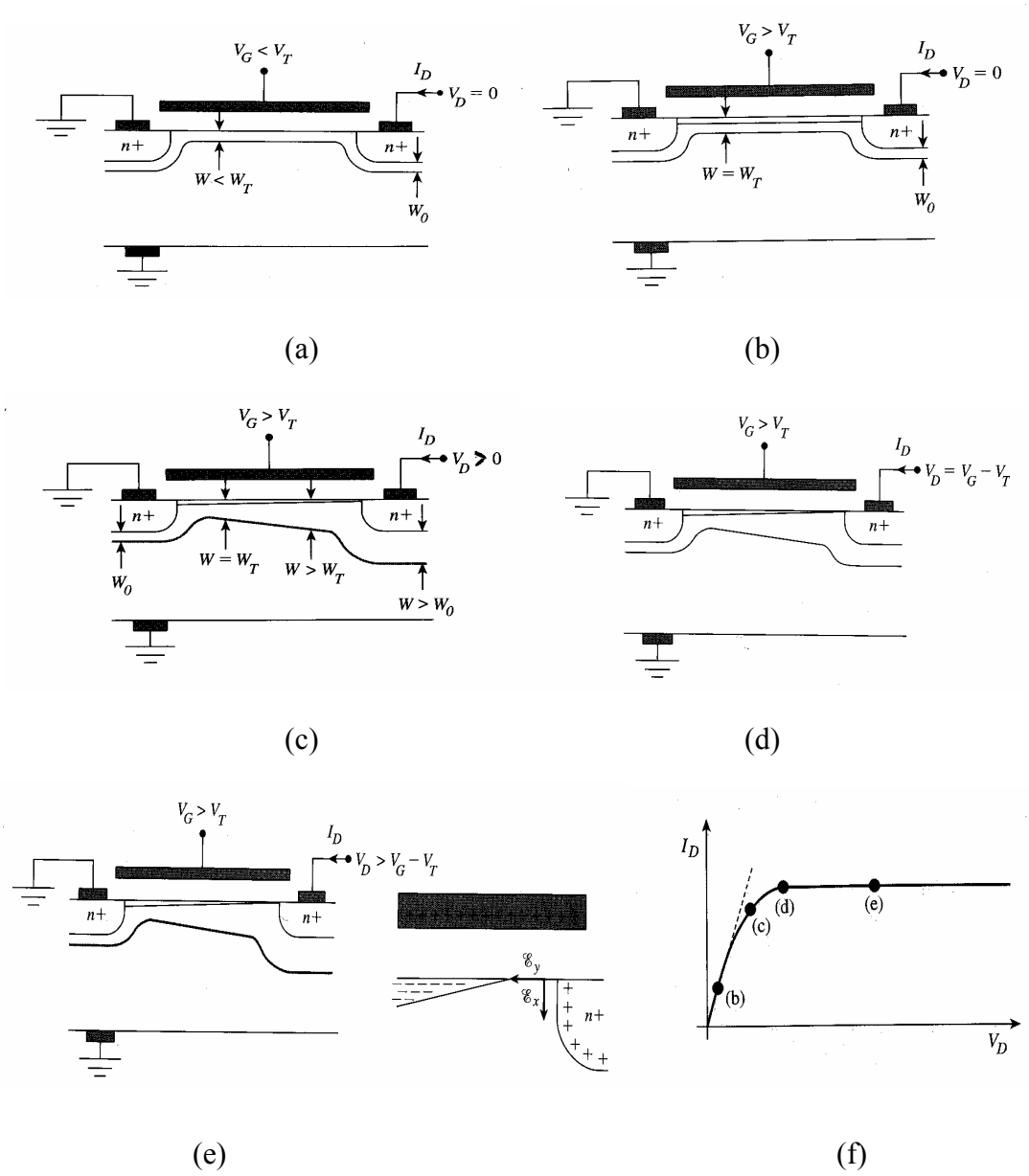


Figure 1.3 MOSFET cross-section for various gate and drain voltages. (a) below threshold; b) above threshold; c) with $V_G > V_T$, $V_D > 0$; d) at initial pinch-off; (e) above pinch-off; (f) I-V characteristics [1].

Recently, TFTs became important electronic devices as addressing switches for flat-panel displays [2]. Among various flat panel displays, the dominant product on the market is the liquid crystal display (LCD). There are two types of LCDs: passive and active-matrix. In a passive-matrix LCD, the state of each pixel is directly controlled by the row and column addressing lines with no active element at the pixel. The advantage of the passive-matrix LCDs is low cost. In an active-matrix LCD, a TFT switching element is formed at the intersection of each row and column addressing line as shown in Fig. 1.4. Each pixel is equivalent to a capacitor (shown in the figure as two parallel capacitors), and the charge on this capacitor is controlled through the TFT. Two capacitors are used in this display to improve the retention characteristics of the signal charge. The advantages of the active-matrix LCDs are large-area, high-resolution, and fast response time. Because of these advantages, active-matrix displays dominate the marketplace.

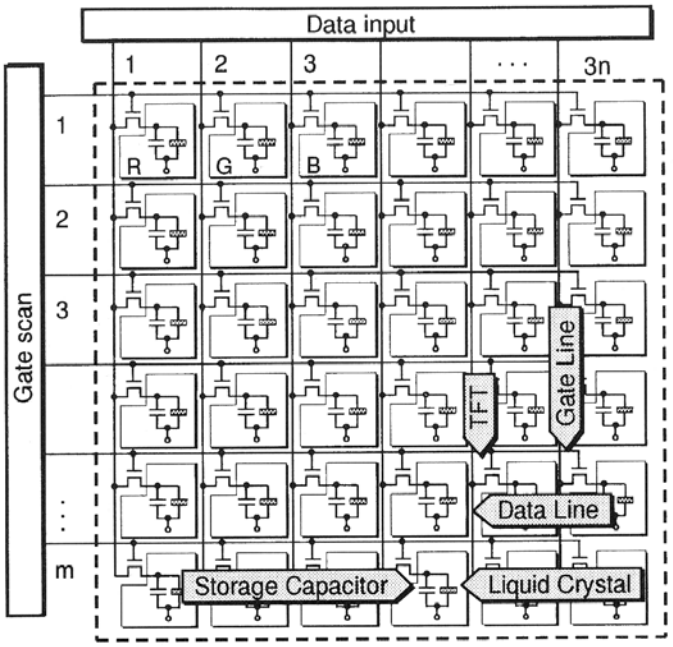


Figure 1.4 A schematic diagram of a TFT-LCD [3].

For active-matrix LCDs, either amorphous or polycrystalline silicon is used as the semiconductor for the TFTs. Hydrogenated amorphous silicon is particularly well suited because it can easily be deposited over large areas at a low temperature (250°C) that is fully compatible with the glass used for the displays [3]. In addition, it has a high resistivity, leading to TFTs with low leakage currents [4]. A thin film of silicon is deposited on the top of a glass, and the TFTs are fabricated from the thin film layer using standard photolithography techniques that are adapted for the large areas involved. Because of the large demand for these displays, an industry has developed to produce arrays of TFTs on glass substrates relatively cheaply. As such, these arrays can now be used for other products besides liquid crystal displays.

1.2 Applications of a-Si:H TFTs

The arrays of a-Si:H TFTs commonly used in active-matrix LCDs are also used for large-area, flat-panel X-ray detectors for medical imaging [5][6][7] and other detectors requiring TFTs over a large area. Here, I focus on the X-ray detectors since these provide the impetus for my thesis research.

1.2.1 Active Matrix Flat Panel Imagers

In a flat-panel X-ray detector, the whole X-ray image is captured and then converted into a digital form [8]. Flat-panel X-ray detectors are classified into two types depending on how the X-rays are detected: indirect conversion or direct conversion as shown in Fig. 1.5. The indirect conversion X-ray detector is composed of a scintillator, a light-sensitive photodiode and a TFT array, while the direct conversion X-ray detector includes an X-ray sensitive photoconductor and a TFT array [9]. In the indirect X-ray detectors, X-ray photons are converted into visible light in the scintillator layer, and then the photodiodes transform the visible light into electrical

charge, and the TFT array reads out the electrical charge. The system is composed of the sensor-array, the readout and the amplifiers; the sensor-array consists of a matrix of a-Si photodiodes, the readout includes the TFTs and the column addressing electronics [10]. Fig. 1.6 shows the schematic diagram of several pixels from an indirect conversion system; notice how the TFTs are used to gate the photodiodes. In the indirect X-ray detector, lateral diffusion of light leads to reduced sharpness and reduced spatial resolution of the image. Fig. 1.7 shows different examples of lateral diffusion: (a) in nonstructured indirect X-ray conversion detectors, (b) in the indirect X-ray detectors with structured scintillator layer, and for comparison (c) in the direct X-ray detectors discussed below. In order to overcome this disadvantage, some indirect X-ray detectors employ structured scintillators that are composed of cesium iodide crystals grown perpendicularly to the detector surface. The single crystals have a diameter of about 5 to 10 μm and considerably reduce the lateral diffusion of the scintillator light [6].

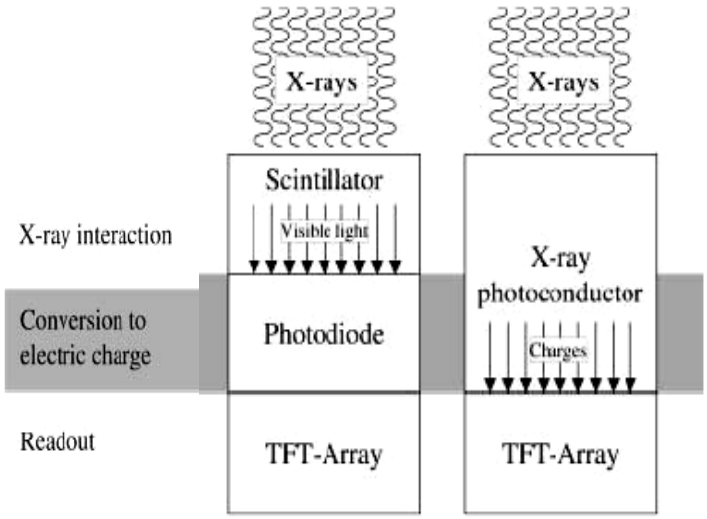


Figure 1.5 The different types of X-ray detectors: (a) indirect (b) direct [6].

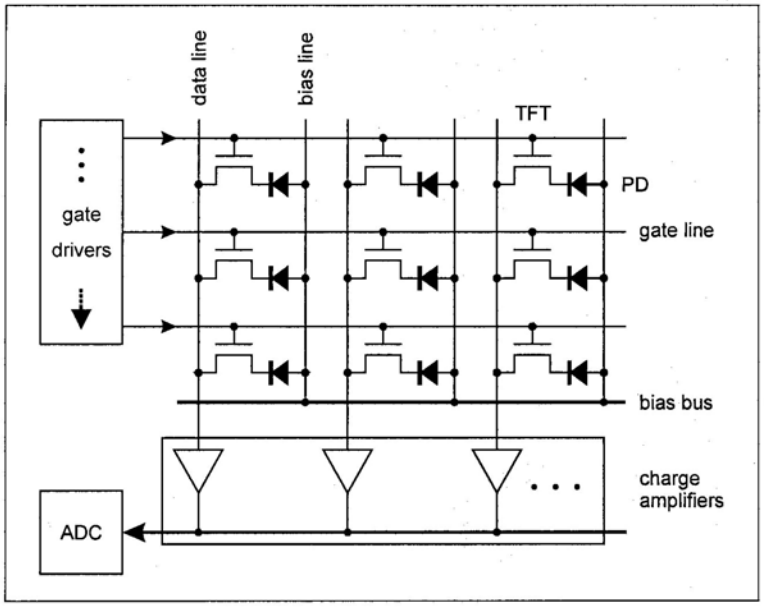


Figure 1.6 The block diagram of an indirect system arrayed with TFTs and photodiodes [10].

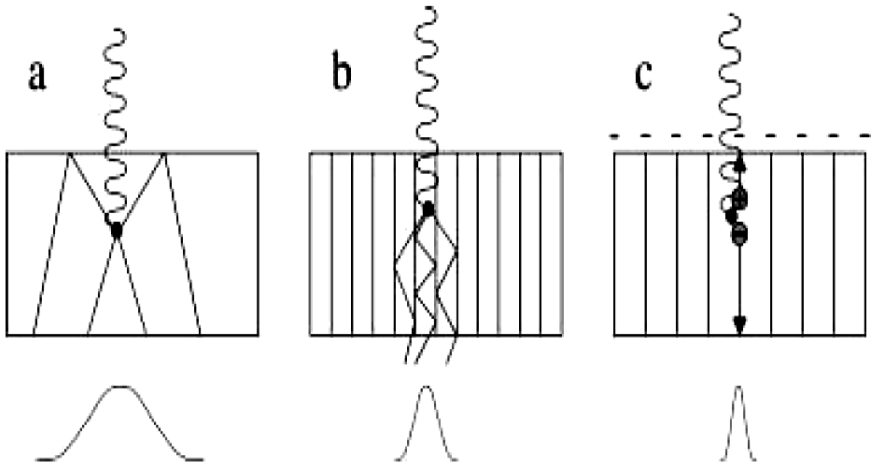


Figure 1.7 Different examples of lateral light diffusion [6].

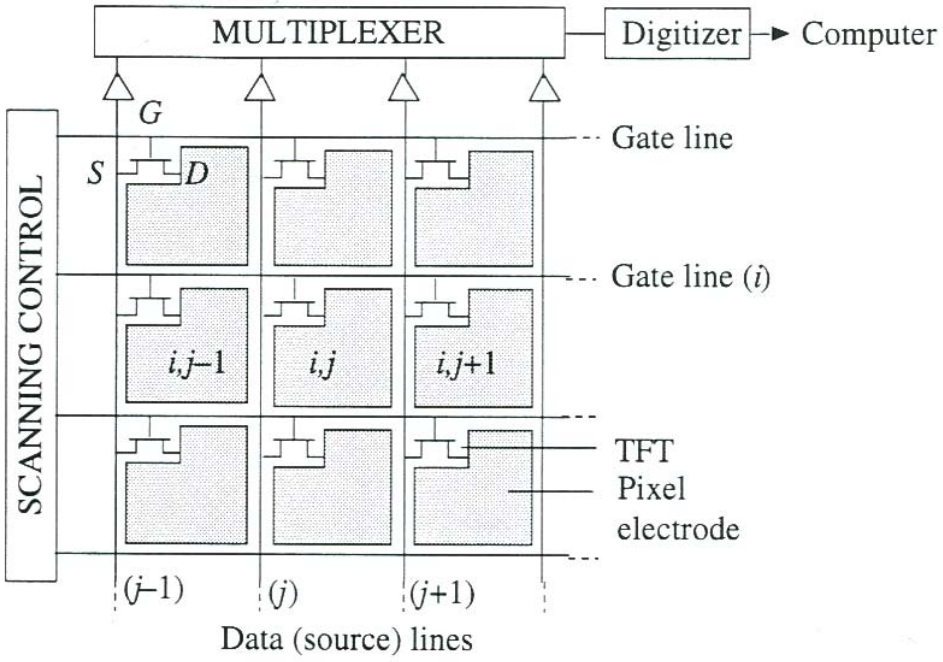


Figure 1.8 The block diagram of a typical TFT array with storage capacitors [11].

In the direct conversion X-ray detectors as shown in Fig. 1.5(b), X-ray photons are converted directly into electrical charge by a photoconductive layer, and the charge is collected and stored on capacitors. The TFT array reads out the stored electrical charge; the collected charge is proportional to the amount of X-rays received by the pixel. Amorphous selenium is typically used as a photoconductor because of its excellent X-ray absorption and very high spatial resolution. As shown in Fig. 1.7(c) and 1.9, the direct conversion detector has much less lateral diffusion because charges move perpendicular to the surface under the influence of the applied electric field [6]. The detector is composed of millions of individual pixel capacitors connected by TFTs (one for each pixel) to charge amplifiers as shown in Fig. 1.8. The operation of the TFT array is as follows. All TFTs in a row have their gates connected, whereas all TFTs in a column have their source connected. When gate line i is activated, all TFTs in that row are turned on, and N data lines from $j = 1$ to N read the charges on the pixel electrodes in row i. The parallel data are multiplexed into a series of charge amplifiers and then digitized and

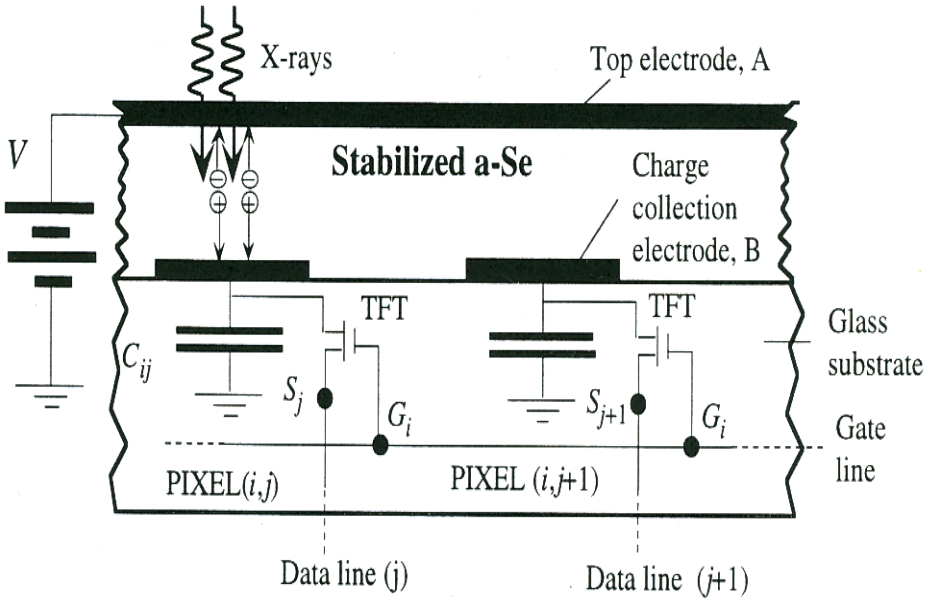


Figure 1.9 Side-view of a direct conversion, flat-panel X-ray image detector [11].

transferred to a computer for imaging. The scanning control activates the next row ($i+1$), and all the pixel charges in this row are read and multiplexed until the whole matrix has been read [11].

1.3 Research Objectives

When an array of hydrogenated amorphous silicon thin film transistors is used as a switching device in a detector, the noise inherent in the a-Si:H TFTs contributes to the overall noise figure of the detector and degrades the signal to noise ratio [12]. In order to properly model such detectors, the noise of the TFTs must be measured, and these measurements are the primary goal of this research. Measurements of low frequency noise ($1/f$ noise) are also a sensitive diagnostic tool for assessing the quality of TFTs. Further, if the measurements lead to a better understanding of the origins of the noise, devices could be designed to reduce the noise level and

as a consequence improve detector quality [13]. This research study examines the characteristics of low frequency noise in a-Si:H TFTs with different channel lengths and how the noise depends on gate voltage and source-drain current; the Hooge's parameter is calculated. In addition, I observe the change of the noise power after gate-voltage stressing. Finally, I incorporate the measurements in a theory of the signal to noise ratio for an indirect x-ray detector.

1.4 Thesis Outline

This thesis is divided into six chapters. Chapter one introduces a-Si:H TFTs and their applications. Chapter two provides the physics and properties of hydrogenated amorphous silicon thin film transistors. Chapter three reviews the types of electrical noise found in devices and briefly introduces the mathematics of noise analysis. Chapter four explains the experimental apparatus and procedures used in this research. Chapter five contains the experimental results and discussions. The final chapter describes the summary and conclusions.

2. THE PHYSICS AND PROPERTIES OF a-Si:H TFTs

This chapter introduces the physics of amorphous silicon and the properties of a-Si:H TFTs. The literature describing amorphous semiconductors is vast; I concentrate on those aspects relevant to understanding the fabrication and operation of the TFTs including the structure of amorphous materials, a method for depositing a-Si:H, the density of states (DOS), and metastable phenomena that occur in a-Si:H. Different TFT structures are described in the next part. In the last part, I explain the static and dynamic characteristics and the threshold voltage shift in a-Si:H TFTs.

2.1 The Basic Properties of Amorphous Silicon

The disorder of the atomic structure is the main characteristic that distinguishes amorphous from crystalline semiconductors. The structural disorder affects the electronic properties in different ways. The disorder, characterized by deviations in the bond lengths and bond angles, changes the electron density of states and affects both electron and hole localization and causes a strong scattering of the carriers. Structural defects like broken bonds have corresponding electronic states. The possibility of alternative bonding configurations of each atom leads to a strong interaction of both electronic and structural states and causes the phenomenon of metastability [3]. Research on amorphous silicon began with pure material without hydrogen. Unhydrogenated amorphous silicon has a high defect density that prevents doping, photoconductivity, and the other desirable characteristics of a useful semiconductor. Adding

hydrogen improves the material by removing most of the defect states and leads to high photoconductivity, low defect density, and doping [14].

2.1.1 Growth and Atomic Structure

Most of the characteristics of the a-Si:H structure and electronic properties are defined by the growth conditions and depend on the deposition process. The usual method of depositing a-Si:H is by plasma decomposition of silane gas (SiH_4) with other gases added for doping and alloying. Fig. 2.1 shows a typical plasma chemical vapor deposition system to deposit a-Si:H and silicon nitride thin films. The diode type reactor contains two parallel-plate electrodes; rf power is applied to one electrode and the substrates are attached to the other one. The rf power decomposes the silane into various radicals (including SiH_3 and SiH_2) and forms a plasma. The radicals that reach the substrates undergo chemical reactions at the surface that result in the formation of the a-Si:H layer. If ammonia gas (NH_3) or nitrogen gas (N_2) is added to the silane then a silicon nitride layer is deposited, or if small quantities of phosphine (PH_3) or diborane (B_2H_6) are added, n-type or p-type a-Si:H respectively results. By using this technique, films can be deposited up to several microns in thickness with thickness variations of only a few percent or less over the entire surface area. Hydrogen is also incorporated in the growing film because the substrate temperature is relatively low (250°C), and so amorphous silicon contains considerable quantities of hydrogen (10-30 at.%). The material is called hydrogenated amorphous silicon (a-Si:H) to emphasize that it is in fact an alloy of hydrogen and silicon. The hydrogen is highly advantageous because it passivates the dangling bonds that are inevitably present in the silicon random network [1][3].

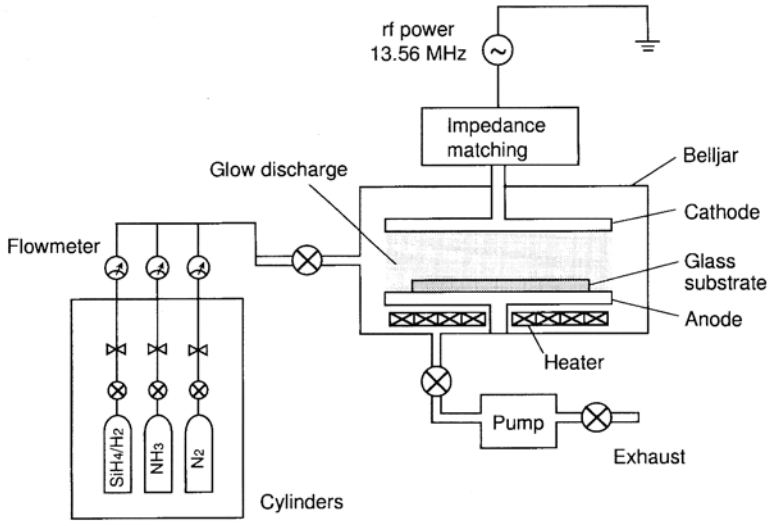


Figure 2.1 The plasma CVD system to deposit thin film of hydrogenated amorphous silicon and silicon nitride [1].

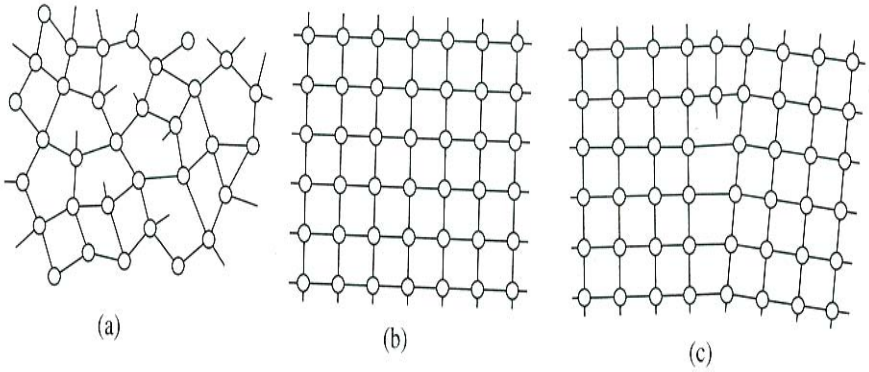


Figure 2.2 Different atomic structures: (a) amorphous, (b) crystalline, and (c) polycrystalline materials [1].

The material deposited under these conditions has no long-range crystalline order (Fig. 2.2a), and thus it is different from single crystal materials (Fig. 2.2b) and polycrystalline materials (Fig. 2.2c). Amorphous silicon is described as a random network with a distribution of bond angles. Fig. 2.2a shows a two-dimensional idealization of the amorphous-silicon structure. In the three dimensions, a random network connecting five- or six-membered rings exists [1].

2.1.2 The Electronic Density of States

The distinction between localized and extended electronic states is one of the fundamental concepts in the study of amorphous semiconductors. A localized state is one in which the wavefunction of the electron decays exponentially away from a particular site and thus the electron is not capable of moving freely through the material. An ideal crystal does not have localized states but due to the disorder present in amorphous materials, localized states occur. The localized states include two different types: deep states and band tails. As shown in Fig 2.3b, the band edges of a crystal are replaced by band tails of states due to variations of the bond lengths and angles. Some of the tail states become localized; the extended and localized states are divided by the mobility edges at energy E_C for the conduction band tail and E_V for the valence band tail. Only electrons above E_C or holes below E_V are mobile and contribute to conduction at zero temperature. The locations of the mobility edges depend on the degree of disorder. The band tails control electronic transport at the mobility edge because the mobile charge carriers are continuously being trapped into tail states for periods of time resulting in a decrease in their effective mobility. The deep (near the center of the mobility gap) defect states originate from defects in the amorphous silicon network particularly dangling bonds. These defects control electronic properties through trapping and recombination.

There are several possible conduction mechanisms in an amorphous semiconductor: extended state conduction by thermal activation of carriers from the Fermi energy (E_F) to above the mobility edge, band tail conduction by hopping from site to site within the tails, and hopping conduction at the Fermi energy. The latter mechanism requires that the density of states is large enough for significant tunneling of electrons. Since the states at E_F are usually defect states, Fermi level hopping is important for very defective material. When hydrogen is added to amorphous silicon, the defect density is reduced (typically below 10^{16} $cm^{-3}eV^{-1}$ for undoped a-

Si:H) and the Fermi energy hopping conduction is suppressed. Although the above three mechanism are observed in a-Si:H (LeComber and Spear 1970), at room temperature the extended conduction near the mobility edge is dominant. The conductivity is a macroscopic quantity representing an average property of the carriers as they move. The calculation of the conductivity includes the transfer rate, and scattering and trapping processes. Even though conductivity near the mobility edge in disordered materials has been discussed for many years, a complete theory is not agreed upon. Generally the conductivity is expressed as the product of the carrier density and the carrier mobility [1] [14]. The minimum room temperature conductivity in undoped a-Si:H is typically 10^{-10} to 10^{-12} $(\Omega cm)^{-1}$; the conductivity of heavily doped material can be as high as 10^{-2} to 10^{-3} $(\Omega cm)^{-1}$ [1].

The energy gap of a-Si:H is greater than that of single-crystal silicon and increases with hydrogen content. It ranges between 1.6 eV to 2.0 eV for hydrogenated amorphous silicon; for reference the energy gap for amorphous silicon without hydrogen is between 1.2 eV and 1.4 eV [1].

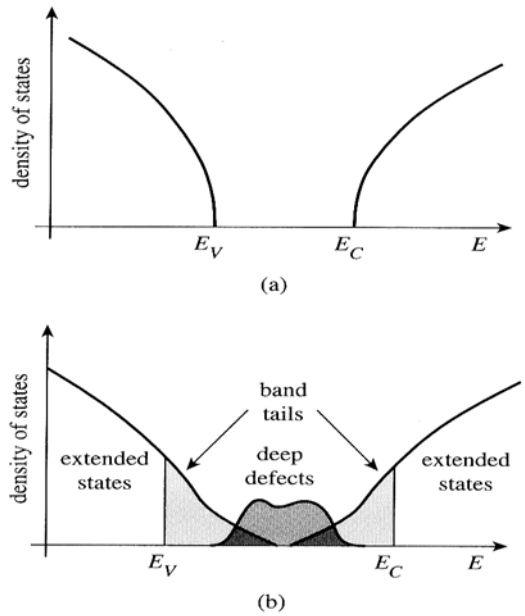


Figure 2.3 Density of states: in (a) single-crystal material and (b) amorphous material [1].

2.1.3 The Metastability of a-Si:H

The phenomenon of metastability occurs when an external excitation such as illumination, current injection, or charge accumulation at interfaces causes a reversible change in a measured quantity such as conductivity. For example, upon illumination the conductivity of lightly doped a-Si:H decreases and the number of dangling bonds, measured by electron spin resonance increases. These changes can be reversed by annealing to 150 -200°C. The current theory of metastability in a-Si:H uses the language of solid state chemistry; the changes are viewed as reactions that change the bonding and charge states of various atoms. The equilibrium concentration of atoms in each bonding configuration and charge state depends on the temperature but also on the Fermi level since electrons usually mediate the reactions. Any process causing the Fermi energy to change alters the equilibrium of the states and tends to change their density. This effect is important for FETs since the electron accumulation layer is a region in which the Fermi level is shifted toward the conduction band. This shift results in the creation of defects in the a-Si:H resulting in a slow change to the transfer characteristics (source-drain current versus gate voltage) of the FET while the transistor is held on with a large accumulation charge. The change of interface defect density (ΔN cm^{-2}) causes a shift of threshold voltage by $\Delta V = e\Delta N / C_g$ where C_g is the capacitance of the gate dielectric [14]. When first observed, researchers interpreted the threshold shift as due to charge trapping in the gate insulator; however, it became clear that defect creation in the a-Si:H film near the interface was responsible for most of the shift. I will discuss the shift of threshold voltage in more detail below.

2.2 Amorphous Silicon TFTs

A TFT differs from a typical MOSFET in that it is composed of very thin layers deposited on an insulating substrate, whereas most MOSFETs are formed from a semiconductor wafer as mentioned in chapter one. Amorphous silicon TFTs are fabricated from a thin layer of a-Si:H. a-Si:H is particularly suited for TFTs in LCDs because it can be deposited over large area and at low temperatures. Also, the carrier mobility of a-Si:H is just enough to charge the pixel's capacitor, and the off-current of the TFT is sufficiently small so that the capacitor is not discharged during the frame time [3].

2.2.1 The Fabrication of Amorphous Silicon TFTs

Amorphous silicon thin film transistors are fabricated in a variety of structures. Fig. 2.4 shows four TFT structures that differ in the ordering of the various layers: active layer, gate insulator, source-drain contacts, and gate electrode. In a coplanar TFT, drain, source, and gate electrodes are on the same side of the semiconductor film. In a staggered TFT, source and drain are on the side of the semiconductor nearest the substrate and the gate is on the opposite side of the semiconductor. In an inverted staggered TFT, the gate is deposited on the substrate first, and the gate insulator, active layer, and source-drain contacts are sequentially deposited. Finally, an inverted coplanar TFT reverses the order of the active layer and the source-drain contacts. The inverted-staggered a-Si:H TFT is widely used in LCDs. There are two common bottom-gate a-Si:H TFT structures, the back-channel-etched (BCE) a-Si:H TFT and the etch-stopper (ES) a-Si:H TFT as shown in Fig. 2.5. In the BCE structure, gate, gate insulator, active layer, and n^+ a-Si are continually deposited, and then the n^+ is etched from the channel region of the transistor. In the ES structure, gate, gate insulator, active layer, and a second silicon nitride layer (stopper) are deposited, and then the second silicon nitride is etched from the contact

regions before depositing the n^+ layer. The BCE TFT requires a minimum of three mask steps; the ES TFT requires a minimum of four mask steps. Many LCD companies are adopting a BCE a-Si:H TFT due to the simpler fabrication process [15][16].

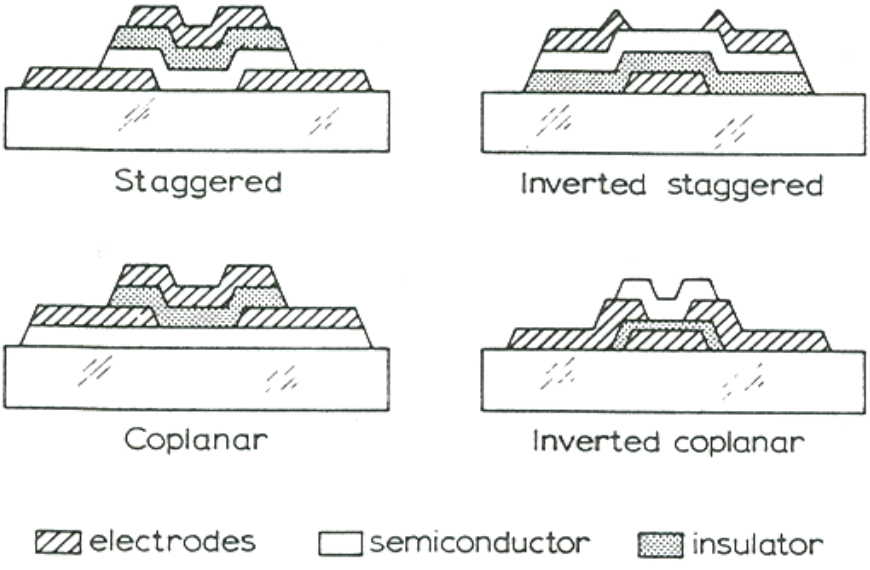
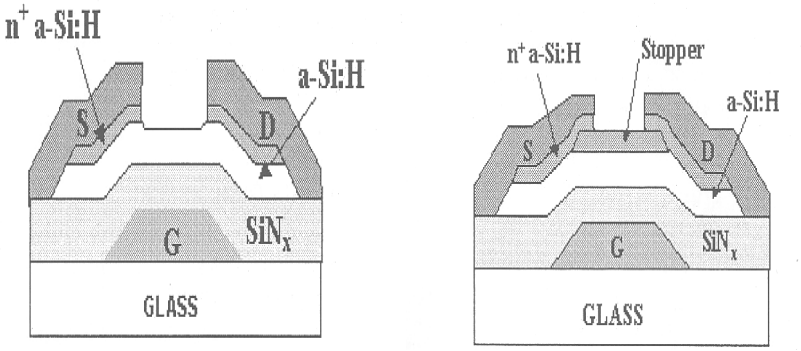


Figure 2.4 TFT configurations [15].



(a) (b)

Figure 2.5 The inverted-staggered a-Si:H TFT structures [16].

2.2.2 The Characteristics of a-Si:H TFTs

2.2.2.1 Static Transistor Characteristics

An a-Si:H TFT and a standard MOSFET or JFET have similar drain curves consisting of a linear region and a saturation region. The drain-source current increases linearly with drain voltage ($V_D << V_G$) in the linear region, while the drain-source current is almost constant with increasing drain voltage in the saturated region. Compared to other FETs, the a-Si:H TFT have a higher pinch-off voltage [16].

However, the device physics for the a-Si:H TFTs differs from that of typical MOSFETs due to the presence of localized states in the mobility gap. Fig. 2.6 shows the band-bending and the occupancy of the electronic states for several applied gate voltages. For zero gate voltage, the energy bands are close to the flat band condition and the Fermi level is close to mid-gap. The off resistance is due to the high intrinsic resistivity of a-Si:H and not due to the pn junctions found in typical MOSFETs. When a positive gate voltage less than the threshold voltage is applied, the energy bands bend downward, and the Fermi level moves up through the deep states. Most of the charge attracted to the gate fills these deep states and little is located in the band-tail states or above the mobility edge. The source-drain current increases initially by a small amount due to the small fraction of the electrons above the conduction band mobility edge. The space charge in the deep states increase in proportion to the increase of gate voltage, but the current increases exponentially as the band bending increases. When the gate voltage above the threshold voltage is applied, the space charge in the band-tail states exceeds that in the deep states, even though the Fermi level is still below the tail states. Both the total space charge and the source-drain current increase linearly with gate voltage [15].

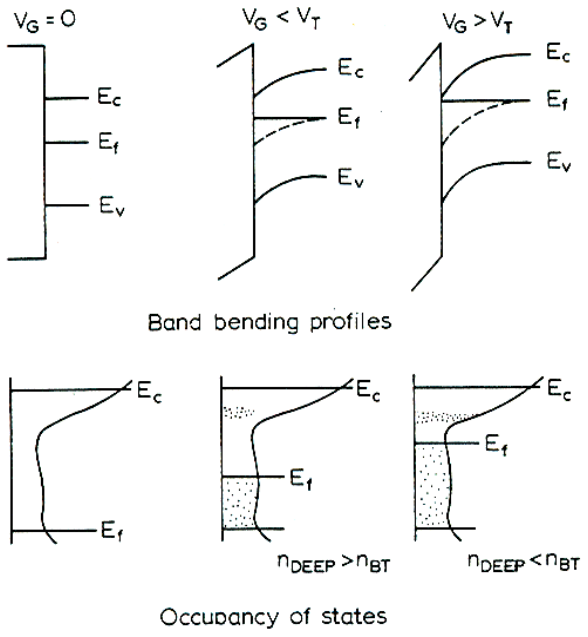


Figure 2.6 The basic operation of an a-Si:H TFTs [15].

2.2.2.2 Dynamic Transistor Characteristics

TFTs act as a switch in most applications; the transistors are typically switched on for tens of microseconds and then switched off for tens of milliseconds. The behaviour of the transistor in this time interval defines the dynamic characteristics. When a positive gate voltage is applied, two distinct processes occur before a steady state develops. First, electrons are injected from the drain-source contacts into the channel region. Second, injected electrons are trapped into the deep localized states. This trapping (or thermalization) process continues until either all deep states are full or thermal emission from the states equals the trapping [17]. Fig. 2.7 shows the changes to the band bending during turn-on. In Fig. 2.7a the dashed lines are the flat-band positions and solid lines are the band bending during the initial deep state trapping, and the solid lines in Fig. 2.7b show the equilibrium situation. Shortly after switch on, the deep states start to trap charge, but the rate of trapping is much higher near the gate insulator interface (region 1)

because of the much higher density of free carriers. Thermal equilibrium occupancy of the deep states is established in that region. However, trapping of free carriers in region 2 continues, and electrons are transferred from region 1 to region 2 resulting in a changing band-bending profile as shown in Fig. 2.7b. The time required for this redistribution of charge takes between 1 μs and 10 s. The changing charge distribution results in an effective dynamic threshold voltage shift [15].

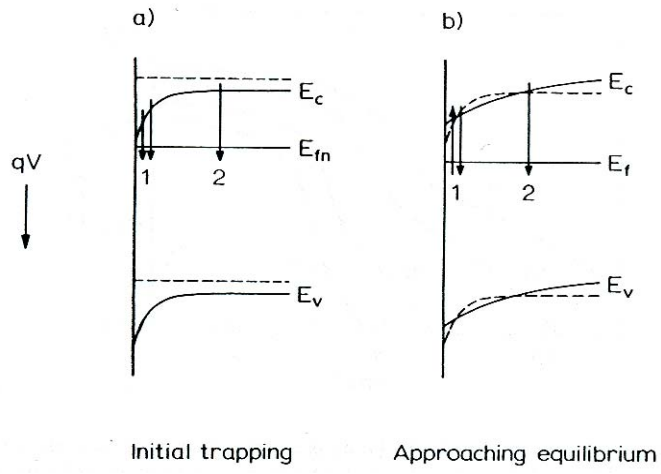


Figure 2.7 The thermalization process: (a) initial trapping and (b) approaching equilibrium [15].

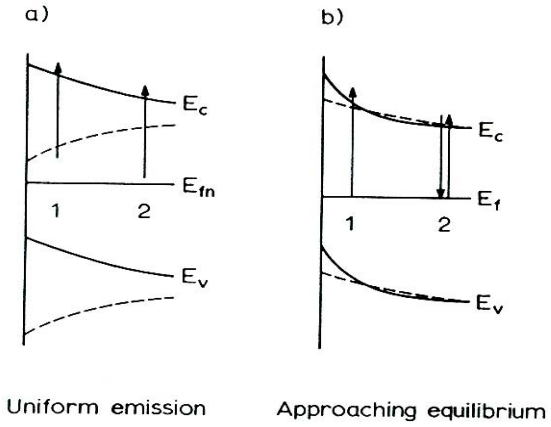


Figure 2.8 The switch-off process: (a) uniform emission and (b) approaching equilibrium [15].

Fig. 2.8 shows the thermal equilibrium band-bending profile before switch-off (dashed lines). If the gate voltage is simply turned off, the trapped electrons must be thermally excited above the mobility edge before they can be swept from the channel region. If the TFT is turned off by applying a negative gate voltage, the energy bands are pushed up, and the band-tail electrons are rapidly swept out to the source and drain contacts. After that, electrons start to emit from the deep states at a rate determined by energy gap. This continues and builds up a uniform space charge in the amorphous silicon until the positive space charge in the silicon equalizes the negative charge on the gate as shown in Fig 2.8a. At this point, thermal equilibrium is established in region 2, but the deep states in region 1 continue to emit and lead to a slow change of charge from region 1 to region 2 in order to change band-bending profile as shown in Fig. 2.8b [15].

2.2.2.3 Threshold Voltage Shift

Applying a gate voltage to a-Si:H TFTs results over time in a change in the transfer characteristics, namely a parallel shift of the I-V characteristics and thus a change in the threshold voltage. The threshold voltage shift depends on the gate voltage, typically as a power law $\pm|V_g|^{\beta}$ where β varies from 1 to 4, but varies only slightly with the drain voltage. Therefore, threshold voltage shift is generally measured under a gate voltage stress with the source and drain electrodes grounded. The threshold voltage can be returned to prestress values by annealing at $200°C$ for 30-60 min [3].

Two models are proposed to explain this threshold voltage shift: charge trapping in the silicon nitride gate insulator and creation of metastable defect states in the amorphous silicon. As shown in Fig. 2.9, when a positive gate voltage is applied, electrons are transferred from the

amorphous silicon to silicon-dangling bond states in the silicon nitride where the charge becomes trapped. Charge trapping in the insulator is strongly field-dependent and requires a relatively high field. The trapped electrons in the silicon nitride act as a permanent charge sheet and screen part of the gate voltage from the semiconductor resulting in a shift to a higher threshold voltage. However, for negative gate voltage, holes tunnel into the insulator creating a positive charge sheet. The positive charge adds to the positive gate voltage producing a shift of the threshold voltage to lower values.

As explained above, whenever the Fermi level changes in a-Si:H, the equilibrium density of dangling bonds changes. Starting with the Fermi level near midgap in intrinsic a-Si:H, a shift of the Fermi level either higher or lower will tend to increase the density of defect states. A larger density of defect states results in a positive shift of the threshold voltage since these states need to be filled to turn the transistor on [17]. Notice that the threshold voltage shifts in the opposite direction for the charge trapping mechanism for negative gate voltage stress and so these two mechanisms can be distinguished experimentally.

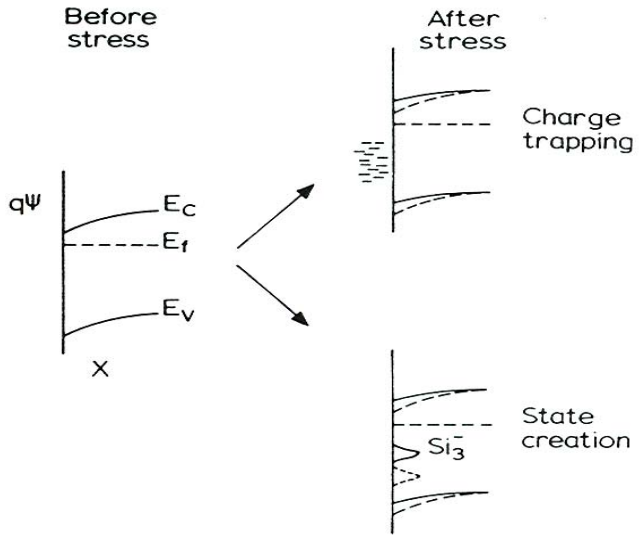


Figure 2.9 Different mechanisms of the charge trapping and state creation [17].

3. ELECTRICAL NOISE

Noise is any unwanted signal that corrupts, reduces the information content of, or interferes with the desired signal. Noise sources can mainly be divided into two groups: intrinsic noise sources and extrinsic noise sources. An intrinsic noise source comes from the fundamental physical in electronic devices, while an extrinsic noise source comes from interactions between a circuit and the surrounding environment [18]. The noise is usually observed as a random fluctuation either in the voltage across the terminals of a device or in the current flowing through the device. This chapter reviews the three most important intrinsic noise sources: thermal noise, shot noise, and $1/f$ noise as well as the mathematics used to describe any noisy process.

3.1 Electronic Noise Sources

3.1.1 Thermal Noise

Thermal noise, commonly known as Johnson noise, comes from the random motion of charge carriers in thermal equilibrium. Charge carriers inside any conducting material are in random motion at a temperature higher than absolute zero. Because the motion is random, at any given time there might be a net accumulation of charge on one side or the other leading to a voltage across the material. Since the thermal noise inherently results from the accumulated motion of many individual charge carriers, it exhibits Gaussion statistics; that is, the histogram of voltages has a Gaussian shape. Nyquist showed that the open circuit RMS voltage produced by a resistance R is given by

$$V_t = \sqrt{4kTBR} \quad \text{(volts rms)} \tag{3.1}$$

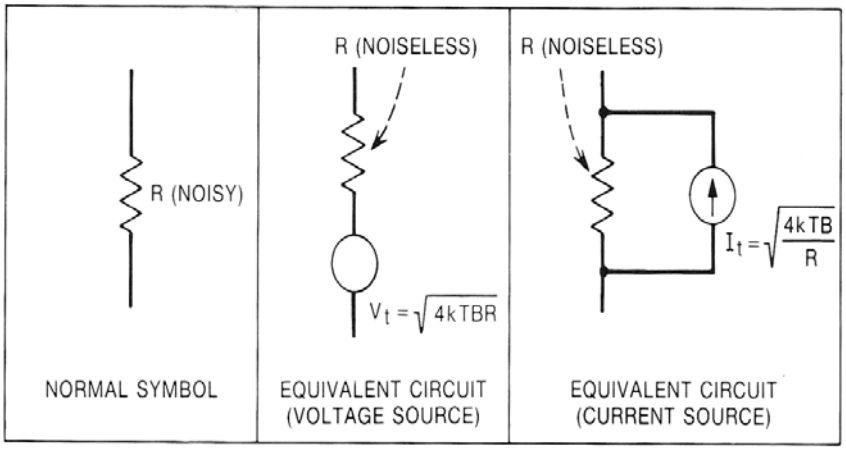


Figure 3.1 Noise models for a physical resistor [19].

where k is Boltmann's constant (1.38×10^{-23} J/°K), T is absolute temperature, B is the bandwidth of the measurement, and R is the resistance [20]. The thermal noise is modeled by replacing the noisy resistor with the combination of a noise-free resistor either in series with a voltage-noise generator or in parallel with a current-noise generator as shown in Fig. 3.1. The current noise generator has a RMS magnitude given by

$$I_t = \sqrt{\frac{4kTB}{R}} \text{ (Amps rms)} \qquad (3.2)$$

In both the voltage-noise and current-noise models, the noise source is a zero mean Gaussian noise generator with a white power spectral density; that is, the spectral density is independent of frequency. In the voltage-noise model, the voltage noise spectral density increases with increasing resistance, whereas in the current-noise model, the current noise spectral density decreases with increasing resistance. Capacitors and inductors do not create thermal noise if they do not have significant resistive components or are suffering from dielectric breakdown. The frequency distribution of thermal noise power is uniform, and thus the noise power is constant for a given bandwidth anywhere in the spectrum. For example, the noise power in a 100-Hz band between 100 and 200 Hz is equal to the noise power in a 100-Hz band between

1,000,000 and 1,000,100 Hz. Such noise with a uniform power distribution in frequency is referred to as "white noise", meaning that it is made up of many frequency components [19].

3.1.2 Shot Noise

Shot noise arises whenever a current is made up of discrete units and the units are statistically independent of each other. Fluctuations in the average current are due to random bunching of the discrete units. An example of shot noise is the current of hailstones hitting a metal roof. Shot noise in an electrical current is often suppressed because any bunching of electrons will tend to spread out due to their mutual Coulomb repulsion. However, if the current is controlled by the electrons either surmounting or tunneling through an energy barrier, then shot noise occurs because the probability of any electron crossing the barrier is independent of the other electrons. Examples of devices with energy barriers include a vacuum tube (between the cathode metal and the vacuum), a pn junction, or a heterogeneous junction like a Schottky diode [19].

Shot noise is modeled as a current noise source in parallel with the device in which the shot noise occurs. The total shot noise is related to the average current (I_{DC}) and is given by

$$I_{shot} = \sqrt{2qI_{DC}B} \text{ (amps)} \qquad (3.3)$$

where q is the charge of an electron (1.6×10^{-19} C) and B is the measurement bandwidth (Hz) [18].

Eq. 3.3 is similar in form to that of thermal noise. The power density for shot noise is also constant in frequency, and the noise has a Gaussian distribution. Dividing Eq. 3.3 by the square root of the bandwidth yields the spectral density

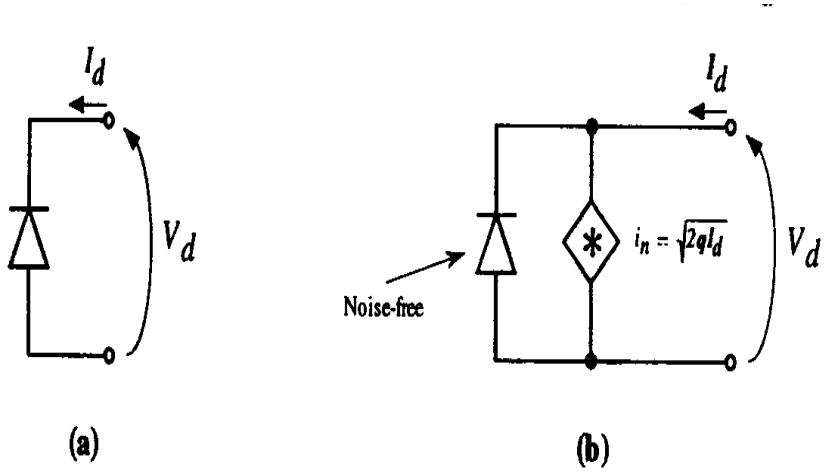


Figure 3.2 Shot and thermal noise in a diode: (a) Diode schematic system. (b) Noise equivalent model [18].

$$\frac{I_{sh}}{\sqrt{B}} = \sqrt{2qI_{dc}} = 5.66 \times 10^{-10} \sqrt{I_{dc}} \tag{3.4}$$

The spectral density is only a function of the dc current flowing through the devices, and thus the amount of shot noise can be accurately determined by measuring the dc current [19].

As an example of shot noise, we can consider the semiconductor diode illustrated in Fig. 3.2(a). The diode has a dc current of I_d and a dc bias voltage of V_d. Fig. 3.2(b) shows the noise equivalent model. A current noise source representing the shot noise in the diode has been placed in parallel with a noise free diode [18].

3.1.3 1/*f* Noise

Excess noise is any noise exceeding the Johnson noise and shot noise [21]. When a constant voltage is applied to a resistor, a fluctuating component of the current is observed in addition to the thermal noise. Similarly, when a constant current flows through a resistor, an excess random fluctuation is observed in the voltage. The size of voltage fluctuations is proportional to

the current and thus what is actually changing is the conductance of the material. These excess noise components show a power spectral density varying as $|f|^{-\alpha}$, where α usually lies between 0.8 and 1.4 and is called 1/*f* noise. For pure 1/*f* noise ($\alpha = 1$), the noise power in any octave is a constant. For example, the noise power between 100 and 200 Hz is equal to the noise power 1,000,000 and 2,000,000 Hz; such noise is sometimes called "pink noise". 1/*f* noise exists in all electronic materials and devices. In the past, 1/*f* noise was variously called excess noise when found in resistors, flicker noise when observed in vacuum tube, and sometimes contact noise although it is well known that 1/f noise is not generally a contact effect. 1/*f* noise is also called low frequency noise because it has increasing spectral power at lower frequencies [19][22]. Johnson first observed 1/*f* noise in an electronic system in 1925 [23], and since then much work on the phenomenon has been done both experimentally and theoretically.

1/*f* noise is ubiquitous and appears not only in measurements of electronic systems but also in odd places such as biological systems and music. The physical origin of 1/*f* noise is not known, except in a few specific cases, and it is impossible to say with certainty whether 1/*f* noise is created at a surface or within the volume of a material. In some cases, it is a surface effect where the semiconductor and oxide interface play an important role; however, in other devices like homogenous resistors, it is regarded as a bulk effect related to a random modulation of the resistance [22].

Three noise models are generally used to analyze 1/*f* noise in MOSFETs: McWhorter's number fluctuation theory [24], Hooge's mobility fluctuation theory [25][26], and a combined model by Hung et al [27][28]. McWhorter's theory states that 1/*f* noise is generated by carrier fluctuation due to the random trapping and detrapping of charge carriers in oxide traps near the

Si-SiO_2 interface. The Hooge model states that 1/*f* noise is created by bulk mobility fluctuations and the power spectral density obeys the empirical formula,

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{S_R(f)}{R^2} = \frac{S_\mu(f)}{\mu^2} = \frac{\alpha_H}{fN} \tag{3.5}$$

where $S_X(f)$ is the spectral density associated with fluctuations of the quantity *X*. The subscripts *I*, *V*, *R*, *G*, and μ refer to current, voltage, resistance, conductance, and mobility noise power, respectively. *N* is the total number of carriers, and α_H is a universal constant. Experimentally, α_H is found to vary from material to material. The combined model by Hung et al proposed that the carrier number fluctuations induce noticeable changes in the surface mobility leading to the 1/*f* noise.

3.2 Mathematics of Noise Analysis and Measurement

Noise is random process and thus any particular time series is unique. Even though we may measure the noise many times, we can not determine precisely what value a noise process will have at any future time. Noise in the time domain can be described using statistical measures such as a mean and variance; the root-mean-square (RMS) of the noise signal is often used. For an observed noise process n(t), the RMS value is defined as

$$n_{rms} = \sqrt{\overline{n^2(t)}} = \sqrt{\frac{1}{T}\int_0^T n^2(t)dt} \tag{3.6}$$

where the horizontal bar indicates a time average. The noise power is proportional to square of the RMS value of the signal.

When two noise sources are added, the instantaneous total signal is the sum of the individual instantaneous values. The total average noise power *N* is

$$\begin{aligned} N &= \overline{n_{total}^2(t)} = \overline{[n_1(t)+n_2(t)]^2} = \overline{n_1^2(t)} + 2\overline{n_1(t)n_2(t)} + \overline{n_2^2(t)} \\ &= \overline{n_1^2(t)} + 2\gamma\sqrt{\overline{n_1^2(t)}}\sqrt{\overline{n_2^2(t)}} + \overline{n_2^2(t)} \end{aligned} \tag{3.7}$$

where γ is the correlation coefficient between the two signals $n_1(t)$ and $n_2(t)$. For uncorrelated noise processes, γ is zero, and the total noise power is the sum of the noise powers in the two signals. If the noise power of the two signals is the same, then the RMS of the total signal is $\sqrt{2}$ larger than the RMS of either signal,

$$n_{total}^{rms} = \sqrt{n_{1\,rms}^2 + n_{2\,rms}^2} = \sqrt{2} n_1^{rms} \tag{3.8}$$

Noise can also be characterized in the frequency-domain; frequency-domain techniques are more informative than time-domain ones for noise analysis. Power spectral density is the most important frequency-domain characteristic of a noise process. Power spectral density is defined as the Fourier transform of the time-domain autocorrelation function. The power spectral density corresponds to the time-averaged noise power per unit bandwidth at the measurement frequency. Therefore, power spectral density has the units of watts-per-Hz. As mentioned above, certain noise spectra have specific names. If the spectrum is flat, the noise is referred to as "white noise". If the spectrum varies inversely with frequency, the noise is pink or is called low frequency noise [19]. If the spectrum is flat at low frequencies but rolls off at high frequencies as f^{-2}, the noise is Lorentzian. In general, there are two ways to measure the noise in the frequency domain. The first is to measure the noise in a very narrow frequency band and move this band through the frequency range of interest. The second is to measure the noise waveform in the time domain and perform Fourier transform analysis to produce the frequency spectrum. The second method is far more efficient.

Understanding the link between experimental observations and the mathematical expressions used to describe stochastic processes is important before undertaking a program of noise measurement [21]. Noise in electronic devices is generally observed as a randomly changing function of time, which is known as a stochastic process. The stochastic process is

characterized by average or statistical properties because its present value cannot be predicted with certainty based on previous values. I consider here only stochastic processes that are statistically stationary meaning their statistical properties are independent of time [22].

The statistical properties of a stochastic process are regular characteristics that become apparent over many trials or observations. A mathematical treatment of such a process can be developed on the basis of an ensemble of statistically similar processes all observed at the same time. For each member of the ensemble, $x^{(1)}(t)$, $x^{(2)}(t)$, … , $x^{(N)}(t)$, a measurement is made and the values are averaged; the statistical properties that result are called ensemble-averaged. Alternatively, a single process can be measured multiple times and those values averaged; the statistics are then called time-averaged [22]. Theory is usually developed using ensemble averages because probability density is more rigorously defined for an ensemble. But ensembles are impractical for experimental work, so measurements use time averaging. However, for stationary processes, ensemble-averaging and time-averaging produce the same results [21].

The statistical property of immediate interest is the power in the noise signal. The derivation starts with Parseval's theorem,

$$\int_{-\infty}^{\infty} x_1(t)x_2^*(t)dt = \frac{1}{2\pi}\int_{\infty}^{\infty} X_1(j\omega)X_2^*(j\omega)d\omega \qquad (3.9)$$

where, $x_1(t)$ and $x_2(t)$ are time functions with Fourier transforms $X_1(j\omega)$ and $X_2(j\omega)$ respectively. The asterisks in Eq. (3.9) represent complex conjugates. The theorem requires that the time functions be absolutely intergrable.

Any real observation will be carried out over a finite period of time. The noise process is observed in the interval $-T/2$ to $T/2$ and the values are assumed zero outside this time

window resulting in the gated signal $x_T(t)$. The time functions in Eq. 3.9 are replaced with $x_T(t)$ as follows

$$\begin{aligned} x_1(t) &= x_T(t+\tau) \\ x_2(t) &= x_T(t) \end{aligned} \tag{3.10}$$

where τ is the delay time. Because $x_T(t)$ is zero outside of its time window, its Fourier transform, $X_T(j\omega)$, exists and from Eq. 3.9 Parseval's theorem provides

$$\int_{-\infty}^{\infty} x_T(t+\tau)x_T(t)dt = \frac{1}{2\pi}\int_{-\infty}^{\infty}\left|X_T(j\omega)\right|^2 \exp(j\omega\tau)d\omega \tag{3.11}$$

where the asterisk on the time function is omitted because $x_T(t)$ is a real process. For $\tau = 0$, Eq. 3.11 simplifies to

$$\int_{-\infty}^{\infty}[x_T(t)]^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty}\left|X_T(j\omega)\right|^2 d\omega \tag{3.12}$$

which is called Plancheral's theorem or the energy theorem. Since power is proportional to $[x_T(t)]^2$, the time integral is proportional to the total energy in the process which is always finite for $T < \infty$. Thus $\left|X_T(j\omega)\right|^2$ can be regarded as the spectral energy density of the noise process with units of energy per Hertz. The average power in the gated noise process is total energy divided by *T*. The power remains finite as $T \to \infty$ for any physical process, so the average power for a non-gated process can be defined as

$$\lim_{T\to\infty}\frac{1}{T}\int_{-\infty}^{\infty}[x_T(t)]^2 dt = \lim_{T\to\infty}\frac{1}{2\pi}\int_0^{\infty}\frac{2\left|X_T(j\omega)\right|^2}{T}d\omega \tag{3.13}$$

where the limits are assumed to exist. The unilateral form is used for the integral on the right since the integrand is an even function of frequency when $x_T(t)$ is real. The $\lim_{T\to\infty}$ and the integral on the right of Eq. 3.13 may be interchanged if an ensemble average is performed first. The unilateral power spectral density of the stationary process $x_T(t)$ is defined as the ensemble average,

$$\overline{S_x(\omega)} = \lim_{T\to\infty} \frac{2\overline{\left|X_T(j\omega)\right|}^2}{T} \tag{3.14}$$

which convergences to a specific value [22].

The expression in Eq. 3.14 shows that the quantity that we want to measure namely the power spectral density is related to the square of the Fourier transform of the signal. However, in an experiment one can not let *T* go to infinity. Instead, the signal is measured for a finite amount of time and then that effectively gated signal is Fourier transformed. Providing that *T* is long enough and that sufficient averaging is done, the resulting power spectrum should closely approximate the theoretical spectrum of Eq. 3.14 [21].

4. EXPERIMENTAL APPARATUS AND PROCEDURE

This chapter describes the sample TFTs, the experimental apparatus and the procedure for performing the noise measurements. The first part concentrates on the structure and I-V characteristics of a-Si:H TFTs used in this research. The second part discusses the experimental apparatus and measurement procedure.

4.1 Device Description

We used a-Si:H TFTs with an inverted-staggered structure that is schematically shown in Fig. 4.1a and b. Fig. 4.1(a) shows the cross section of the TFTs that are fabricated with a standard tri-layer process. Fig. 4.1(b) shows a photomicrograph of fabricated TFTs with different channel lengths (L ~ 23, 33, 50, 80, and 130 μm) but the same channel width (W=100 μm); the gate, source and drain electrodes are clearly visible. Table 4.1 lists the thickness of different layers of the TFT structure. The ratio of width to length is termed as the L:W aspect ratio (or just the aspect ratio). The TFTs with aspect ratios of 0.23, 0.5 and 1.3 are examined in this research. Note that since the width is 100 μm for all devices, the length in μm can be obtained from the aspect ratio by multiplying by 100.

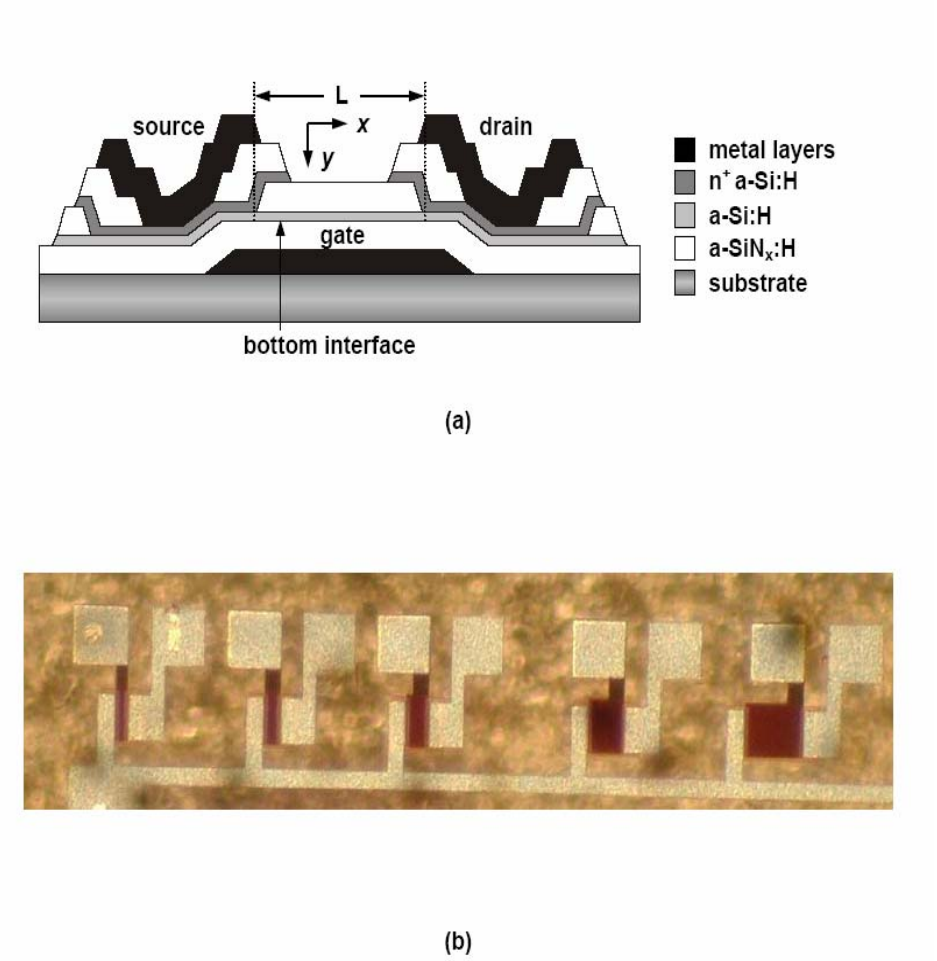


Figure 4.1 Structure of the inverted-staggered TFT. (a) cross section and (b) photomicrograph of TFT samples fabricated with different channel lengths [29].

Table 4.1 Thickness of different layers of the TFT structure [29].

Layer	Thickness (nm)
Gate metal	130
a-SiN_X:H gate dielectric	300
a-Si: H	50
a-SiN_X:H passivation layer	250
n^+a-Si:H contact layer	50
Al metallization layer	500

The TFTs are operated as n-channel, enhancement mode FETs. Fig. 4.2 shows the I-V characteristics of the a-Si:H TFT with 0.5 aspect ratio, that is the drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) for different gate voltages (V_g). The curves clearly show the linear region ($V_{ds} << V_g - V_T$) where I_{ds} is proportional to V_{ds} and the saturated region ($V_{ds} > V_g - V_T$) where I_{ds} is independent of V_{ds}. The threshold voltage (V_T) is 3 V. The I-V characteristics of the TFTs with 0.25 and 1.3 aspect ratios are also similar. In comparison to typical crystalline silicon MOSFETs, a-Si:H TFTs have a larger pinch-off voltage.

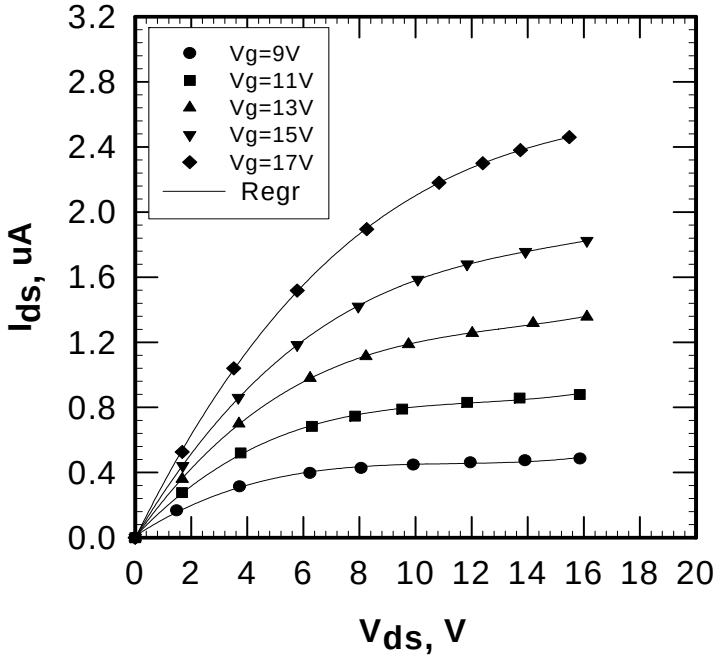


Figure 4.2 The I-V characteristics of the 0.5 aspect ratio TFT for different gate voltages.

4.2 Noise Measurement Techniques

In the experiments described below, I measure the fluctuations in the current passing through the TFT. Therefore, the noise is given as a current noise power density. Following Eq. 3.14, the current noise power density $S_I(f)$ is determined by

$$S_I(f) = 2\frac{\overline{|I_T(f)|^2}}{T} \tag{4.1}$$

where $|I_T(f)|$ is the magnitude of the finite Fourier transform of drain-source current that is measured over a time interval *t*. The bar means an average over many transforms [30].

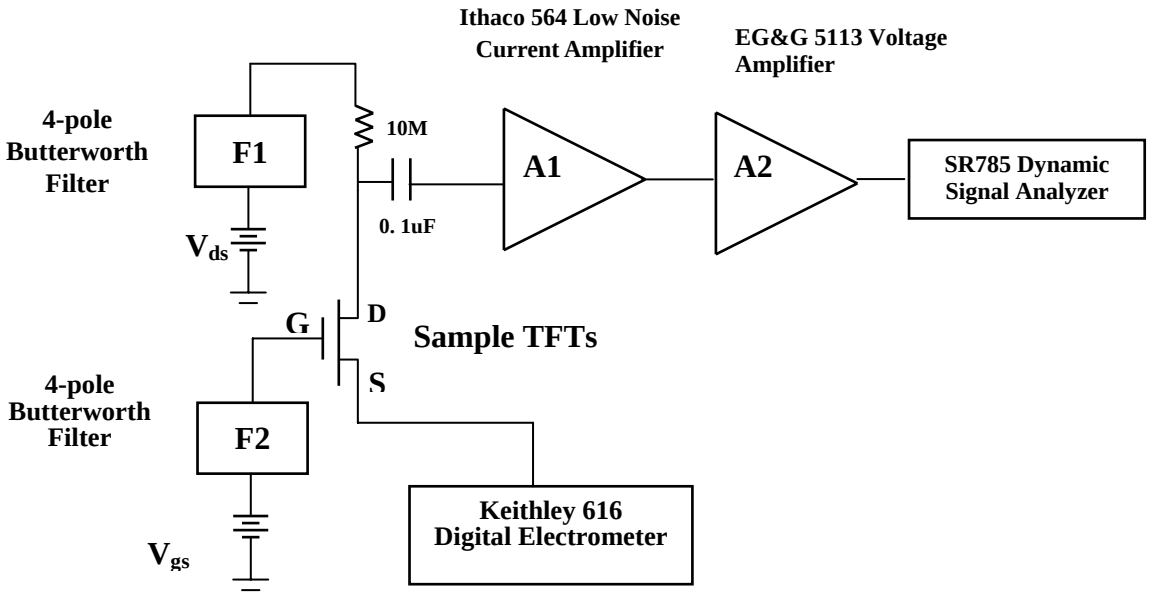


Figure 4.3 The experimental apparatus for noise measurements.

The experimental circuit for the noise measurements is shown in Fig. 4.3. The drain-source voltage supply is connected to drain electrode of the sample TFT through a 10 MΩ resistor, and the gate voltage supply is connected to the gate electrode. A dc blocking capacitor is connected between the 10 MΩ resistor and the drain of the TFT. After the capacitor, an Ithaco 564 low-noise current amplifier (A1) and an EG&G 513 voltage amplifier (A2) are connected in sequence to amplify the noise signal to match the input range of a SR785 dynamic signal analyzer. A Barrison 865B power supply provides the gate voltage, and an Instek pc-3030D dual power supply provides the drain-source voltage. 4-pole butterworth filters with cut-off frequencies of

0.1 Hz for the gate supply and 0.006 Hz for the drain supply are connected between the power supplies and the TFT to insure that no noise from the supplies is injected into the device.

A Keithly 616 digital electrometer is connected to the source of the sample TFT to measure I_{ds}; it is replaced with a short to ground while noise is being measured. This instrument provides current ranges from 10^{-1} to 10^{-11} A with a five-digit display yielding a resolution of 0.1 fA on the most sensitive scale. The accuracy is specified as ±0.5 % of the reading plus +0.1% of the range for the 10^{-1} to 10^{-7} A ranges.

The Ithaco 564 low-noise current amplifier (A1) converts the current fluctuations into a fluctuating voltage with a transimpedance gain selectable in decades from 10^4 to 10^8 V/A. For optimum noise measurement performance, the gain of the amplifier is set to 10^7 V/A in this research. The 564 preamplifier is powered by external batteries in order to minimize the possibility of outside noise. The external batteries are sealed lead-acid type with two 6 V and 12 V batteries connected in sequence to provide ± 18 V. The batteries are contained in a shielded aluminium enclosure and connected to the amplifier through a shielded cable.

The EG&G 5113 voltage amplifier (A2) provides a voltage gain from 1 to 10^5 with an accuracy of ± 2%. The 5113 amplifier contains two filter stages configurable as low pass, high pass, or band pass. However, for the experiments cited herein, the flat response is used which the manufacturer's specifications guaranteed to be flat from DC to 1MHz. The input to the amplifier is always set to AC coupling. The 5113 amplifier is housed in a shielded enclosure and is powered by internal rechargeable batteries. The output of the 5113 amplifier is monitored by an oscilloscope.

The SR785 dynamic signal analyzer, a Fourier Fast Transform (FFT) analyzer, samples the time varying input signal and computes its power density spectrum. Nyquist's theorem says that as long as the sampling rate is greater than twice the highest frequency component of the signal,

the sampled data accurately represent the input signal in the frequency domain. In the SR 785 signal analyzer, the input signal is digitized at 262 kHz. In order to make sure that Nyquist's theorem is satisfied, the input signal passes through an analog anti-aliasing filter, in which all frequency components above 102.4 kHz are removed. The resulting digital time record is then mathematically transformed into a frequency spectrum using a FFT algorithm. The resulting spectrum shows the frequency components of the input signal.

The experimental apparatus operates as follows. The $1/f$ noise appears as fluctuations in the TFT's channel conductance. When a drain-source current is passed through the 10MΩ resistor and the sample TFT, the conductance fluctuations result in fluctuations of the drain-source current. The fluctuations are detected at the midpoint of the resistor divider through the dc blocking capacitor and first amplified by a low-noise trans-impedance amplifier (A1) and then further amplified by a low-noise voltage amplifier (A2). Typical gains are 10^7 V/A for A1 and 100 to 500 for A2. The amplified noise signal is analyzed by the signal analyzer. The signal analyzer digitizes the fluctuating signal and applies a Fourier transform to the resulting time-series to obtain a noise power density spectrum. From 2000 to 5000 spectra are averaged for each run. Prior to any noise measurement, the average dc drain-source current is measured by the electrometer. The sample is rested at least 5 minutes after the gate voltage or the drain-source voltage is changed before the noise is measured to allow the current to stabilize.

As for any noise measuring apparatus, special care is taken to reduce external noise sources from influencing the measurements. Since any fluctuations in either the gate voltage or drain-source voltage produce a spurious noise signal, the power supplies are filtered using 4-pole butterworth filters. This insures that in the frequency rage of interest 1 to 1000 Hz, power supply fluctuations are heavily suppressed. Components used for the 10 MΩ resistor and coupling capacitor are chosen for their low-noise characteristics. The 10 MΩ resistor is

composed of a chain of ten 1 MΩ precision, metal-film resistors; these resistors were previously tested and found to have very low inherent 1/*f* noise. The capacitors are non-polarized, metalized polyester and ceramic types. The amplifiers are battery powered to reduce extraneous signals from the mains.

5. RESULTS AND DISCUSSION

This chapter covers experimental results and data analysis. First, I introduce the normalized noise power spectrum. Second, I observe the effects of gate voltage and channel length on the noise spectrum. Third, I investigate the effects of the drain-source voltage and the drain-source current on the noise spectrum. Fourth, I discuss the effect of gate-biasing time on the noise. Fifth, I calculate Hooge's parameter using both the total number of carriers and the number of free carriers in the channel. Finally, I calculate the signal-to-noise ratio in an array of a-Si:H TFTs and photodiodes

5.1 Normalized Current Noise Power Spectra

I present the experimental noise results as normalized noise power density S_n spectra. S_n is obtained by dividing the current noise power density S_I by the square of the drain-source current. Fig. 5.1 shows the S_I spectra for the 0.5 aspect ratio TFT for four different drain-source currents; the lines are a regression fit of the power law $S_I(10\,\mathrm{Hz})\,f^{-\alpha}$ to the data for each spectrum. Notice that S_I increases as I_{ds}^2; this scaling is a trivial consequence of Ohm's Law and the fact that the $1/f$ noise appears as fluctuations in the drain-source conductance. Since different measurements often use different I_{ds}, comparing S_I spectra is difficult. In order to allow for direct comparisons, I compute the normalized noise power spectra $S_n = S_I / I_{ds}^2$, a quantity that should be independent of I_{ds}. The signal analyzer produces the power spectrum corresponding to the voltage fluctuations at its input, V_{rms}^2. In order to convert to the current

fluctuations in the TFT, the amplifier gains must be taken into account as well as the effective line width of the analyzer. We calculate the TFT's normalized noise power density by

$$S_n(f) = \frac{2V_{rms}^2}{LWG_1^{\,2}G_2^{\,2}I_{ds}^2} \tag{5.1}$$

where LW is the frequency line width of the analyzer, and G_1 and G_2 are the gains of the first and second stage amplifiers, respectively. The factor of 2 is present to convert the values to a single-sided spectrum corresponding to Eq. 3.14.

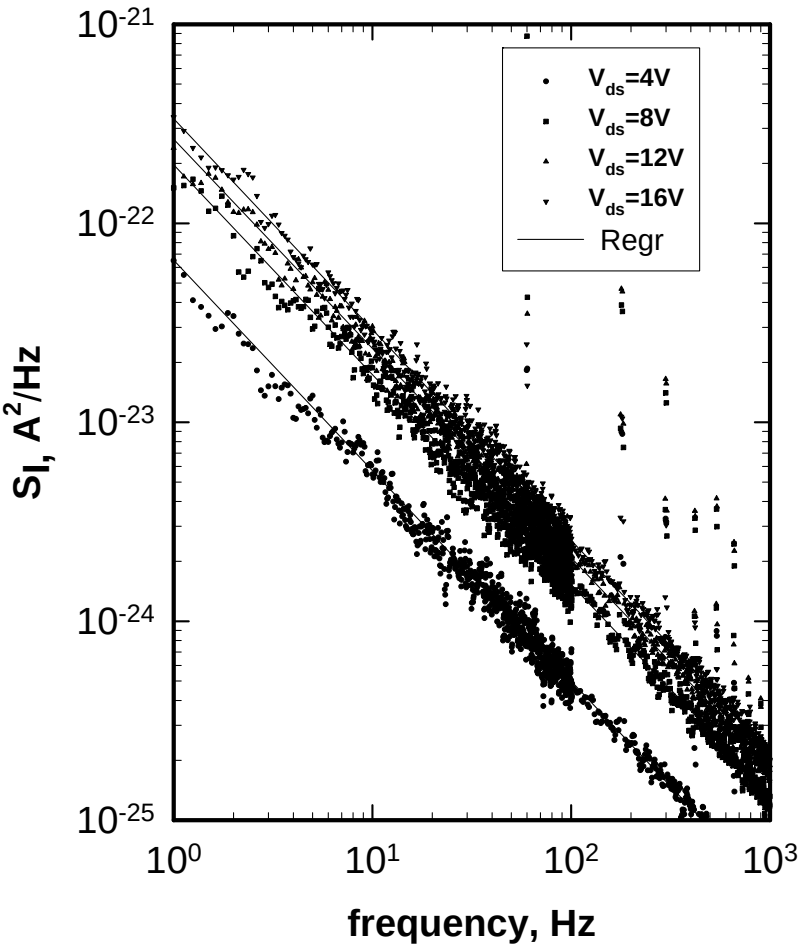


Figure 5.1 Current noise power spectra for the 0.5 aspect ratio TFT.

Fig. 5.2a-c show the normalized noise power spectra over the frequency interval of 1 Hz to 1 KHz for the three TFTs with aspect ratios of 0.23, 0.5 and 1.3 measured using drain-source voltages from 4 V to 16 V and a gate voltage of 13 V. The data for the 0.5 aspect ratio TFT used to generate Fig. 5.2b are the same as for Fig. 5.1. Notice that the normalized noise spectra for the different drain-source voltages lie on top of one another within the scatter of the data, demonstrating that the normalization procedure is correctly accounting for most of the dependence on I_{ds}. However, the regression lines obtained from the data show a small residual dependence on I_{ds} which will be discussed below. Also notice that there is discrete frequency interference at harmonics of 60 Hz. It is impossible to completely eliminate pickup from the mains in spite of our endeavors to reduce extraneous signals. However, these spikes do not interfere with the measurement or analysis of the broadband 1/*f* signal. Similar normalized noise power spectra were obtained for gate voltages of 9 V, 11 V, 15 V and 17 V using the same drain-source voltages.

The power law fits to the data provide two parameters, the slope α and the magnitude of the normalized noise at some frequency which will be taken to be 10 Hz, $S_I(10\,\mathrm{Hz})\,f^{-\alpha}$. The fits for different drain-source voltages give the same α for a given sample to within ±0.005. The fitted αs are almost the same for the TFTs; for the three TFTs $\alpha = 1.06 \pm 0.01$. Since α is very close to one, these devices produce nearly pure, classical 1/*f* noise. This result contrasts with noise measurements of a-Si:H thin films which often yield α values quite different from unity [31]. The magnitude of the normalized noise power at 10 Hz differs between the TFTs; for the 0.23 aspect ratio TFT $S_n(10\,\mathrm{Hz}) = 3\times10^{-11}\,\mathrm{Hz}^{-1}$, for the 0.5 aspect ratio TFT $S_n(10\,\mathrm{Hz}) = 1.5\times10^{-11}\,\mathrm{Hz}^{-1}$, and for the 1.3 aspect ratio TFT $S_n(10\,\mathrm{Hz}) = 5\times10^{-12}\,\mathrm{Hz}^{-1}$ or -105dB, -108dB, and -113dB respectively in engineering units. The magnitude of the

normalized noise power decreases as the channel length increases. I explain the relation between the normalized noise power and the channel length in more detail later.

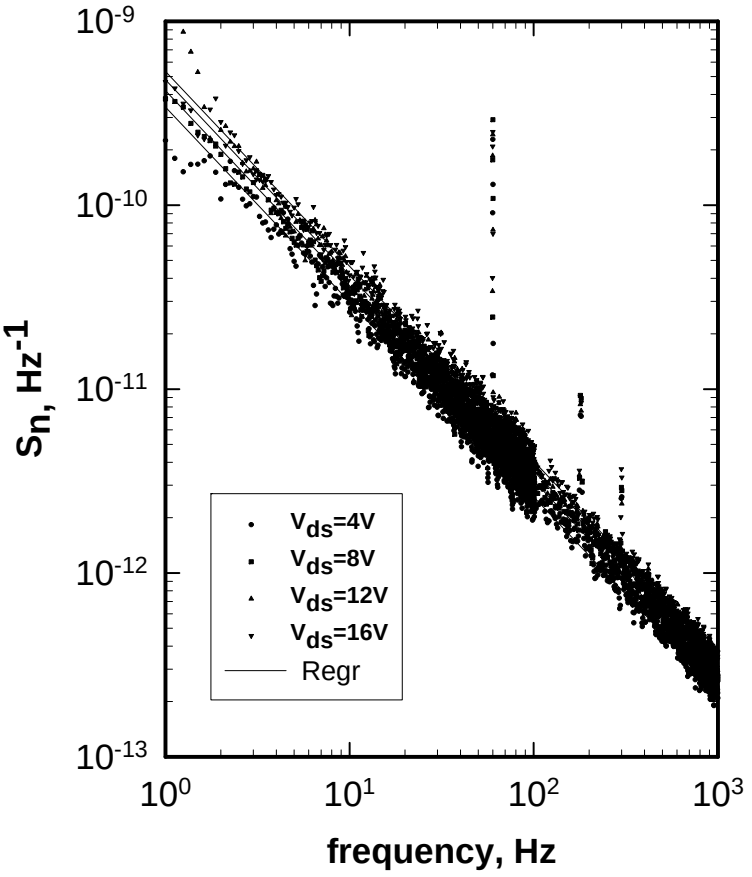


Figure 5.2a Normalized noise power spectra for the 0.23 aspect ratio TFT. V_{ds} and I_{ds} values: 4 V/1.16 μA, 8 V/1.96 μA, 12 V/2.35 μA, 16 V/2.66 μA.

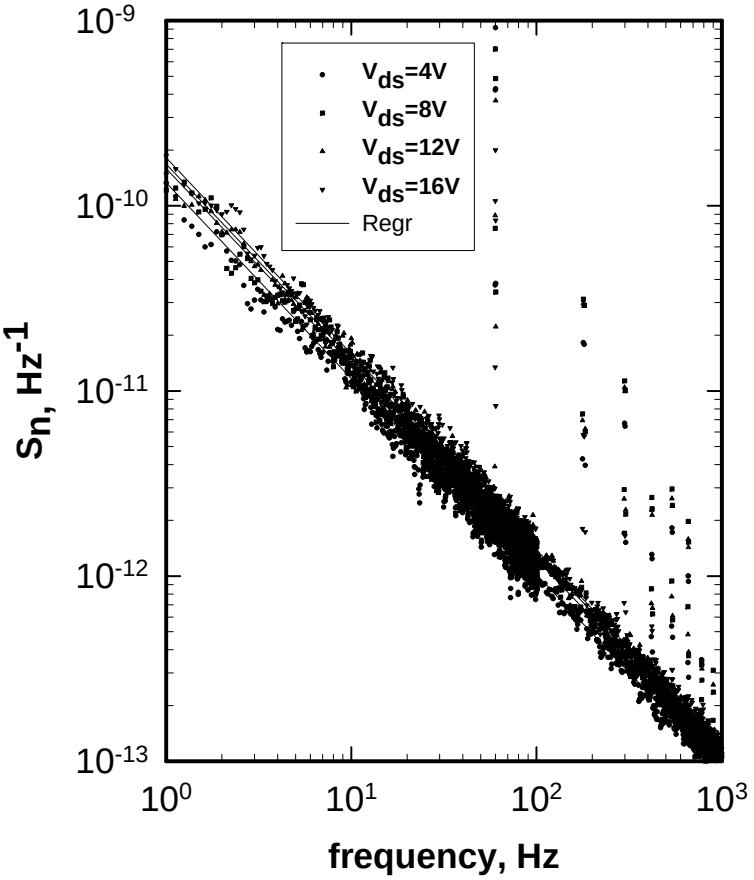


Figure 5.2b Normalized current noise power spectra for the 0.5 aspect ratio TFT. V_{ds} and I_{ds} values: 4 V/0.7 μA, 8 V/1.14 μA, 12 V/1.25 μA, 16 V/1.35 μA.

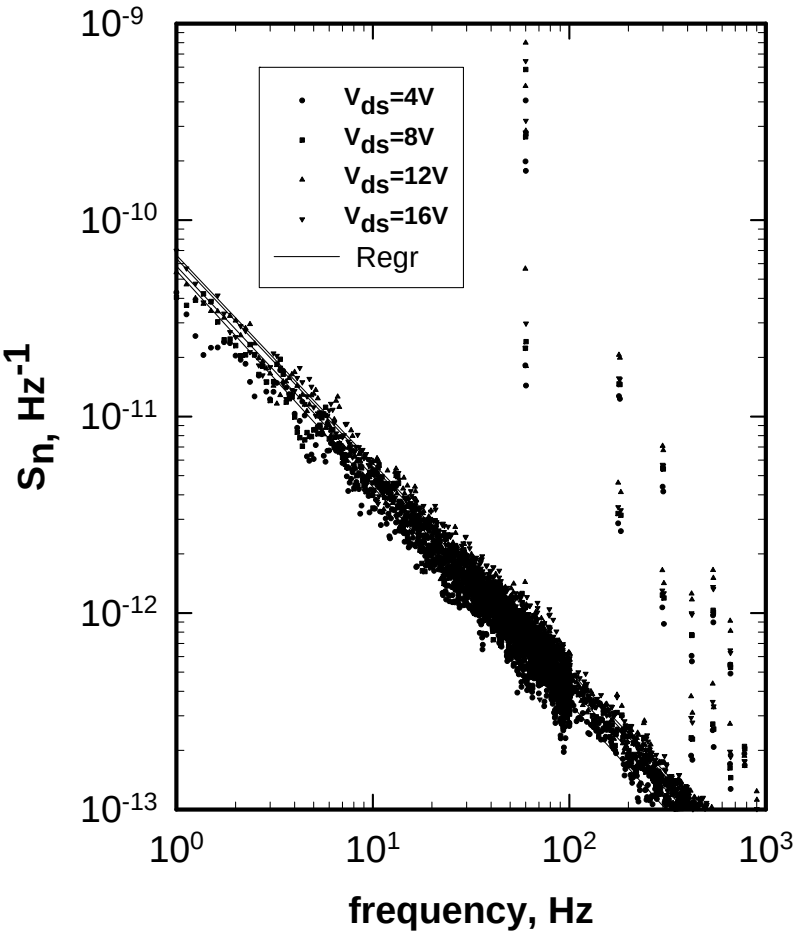


Figure 5.2c Normalized noise power spectra for the 1.3 aspect ratio TFT. V_{ds} and I_{ds} values: 4 V/0.34 μA, 8 V/0.55 μA, 12 V/0.65 μA, and 16 V/0.68 μA.

5.2 The Effects of Gate Voltage and Channel Length

Here, I investigate the relation between the normalized noise power and gate voltage as well as the normalized noise power and channel length. For a homogeneous semiconductor, Hooge suggested the empirical formula [25][32]

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{S_R(f)}{R^2} = \frac{S_G(f)}{G^2} = \frac{S_\mu(f)}{\mu^2} = \frac{\alpha_H}{fN} \tag{5.2}$$

where N is the total number of carriers, α_H is Hooge's noise parameter, and f is frequency. The subscripts I, V, R, G, and μ refer to current, voltage, resistance, conductance, and mobility noise power, respectively. Notice that the quantities on the left of Eq. 5.2 are what we call the normalized noise power density. So Hooge's relation is simply

$$S_n(f) = \frac{\alpha_H}{fN} \tag{5.3}$$

The number of carriers in the channel can be related to the gate capacitance C_g of the TFT by $N = C_g WL(V_g - V_T)/q$ [33] where W and L are the width and the length of the TFT, q is the charge of an electron, and V_g and V_T are the gate voltage and the threshold voltage, respectively. Inserting into Eq. (5.3) yields

$$S_n(f) = \frac{S_I(f)}{I^2} = \frac{q\alpha_H}{C_g(V_g - V_T)WLf} \tag{5.4}$$

Eq. 5.4 demonstrates that the normalized current noise power is inversely proportional to the gate voltage (V_g) and the channel length (L).

The relation in Eq. 5.4 is equivalent to the general relation for bulk generated noise that the magnitude of the normalized noise is inversely proportional to the sample volume and inversely proportional to the number of noise generators. In general, as the gate voltage is increased, the number of carriers in the channel is increased. If the number of carriers in the channel is increased, the conductance is higher,

$$\sigma = nq\mu \tag{5.5}$$

where σ is the conductivity, n is the density of carriers, μ is mobility. If one assumes that $1/f$ noise is caused by N independent carriers, each carrier generating $1/f$ noise then, since the individual noise sources are uncorrelated, the total noise power spectrum S_{GN} due to N carriers can be expressed as

$$S_{GN} = NS_{G1} \tag{5.6}$$

where S_{G1} is the noise power generated by a single carrier. In the same way, the total noise power spectrum generated by the twice as many carriers $2N$ is

$$S_{G2N} = 2NS_{G1} \tag{5.7}$$

However, the normalized noise powers are

$$S_{nN} = \frac{S_{GN}}{G_N^{\ 2}} = \frac{NS_{G1}}{G_N^{\ 2}} \tag{5.8}$$

$$S_{n2N} = \frac{S_{2GN}}{(G_{2N})^2} = \frac{2NS_{G1}}{(2G_N)^2} = \frac{NS_{G1}}{2G_N^{\ 2}} = \frac{1}{2}S_{nN} \tag{5.9}$$

As shown in Eq. 5.9, the normalized noise power decreases in half when the number of carriers doubles. In general, the normalized noise power is proportional to $1/N$ as expressed in the Hooge relation Eq. 5.2. A similar argument shows that increasing the volume of the sample also decreases the normalized noise power in proportion to $1/V$.

5.2.1 The effect of gate voltage on the noise

Fig. 5.3 shows the measured relation between normalized noise magnitude at 10 Hz and the inverse of the gate voltage minus the threshold voltage. The noise values were calculated as follows. For a given gate voltage, noise spectra were measured at several drain-source voltages from 2 V to 16 V. Each spectrum was fit to a power law, and the fit was used to obtain the noise power density at 10 Hz. The noise values for the various drain-source voltages were then averaged together to obtain an average noise power density for that gate voltage. The process was repeated for all the gate voltages 17 V, 15 V, 13 V, 11 V, and 9 V. The experimental results as shown in Fig. 5.3 are in qualitative agreement with the expectation that as the number of carriers in the channel decreases, the normalized noise increases. However, Eq. 5.4 would predict that on a log-log plot the slope should be unity. The slopes of the curves in Fig. 5.3 are 1.54, 1.1 and 0.97 for the 0.23, 0.5 and 1.3 aspect ratio TFTs, respectively. The threshold

voltages of the 0.23, 0.5 and 1.3 aspect ratio TFTs are 3.5 V, 3.0 V, and 1.0 V, respectively and were obtained from the dc characteristics of the TFTs. The larger aspect ratio devices such as 0.5 and 1.3 aspect ratio TFTs are in closer quantitative agreement with Eq. 5.4, while for unknown reasons the 0.23 aspect ratio device produced a slope greater than unity.

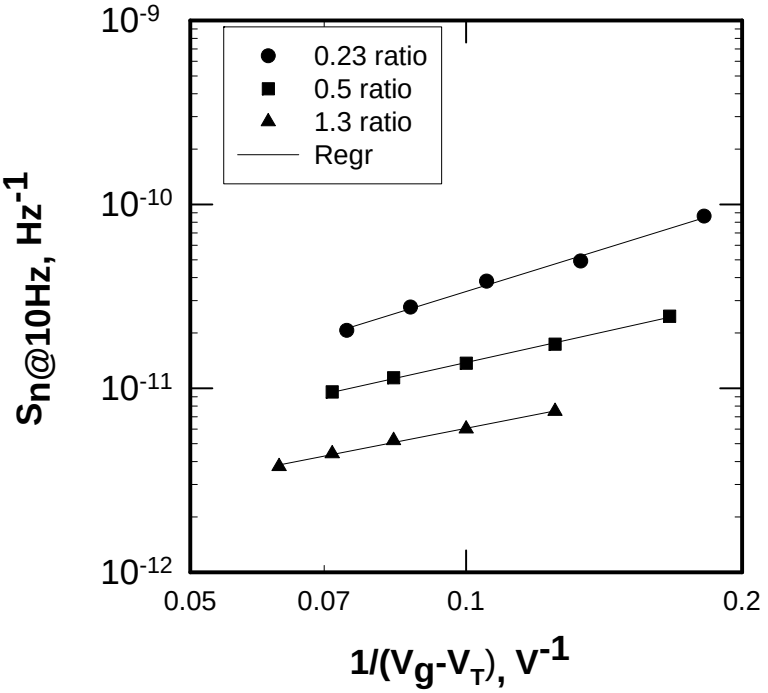


Figure 5.3 S_n at 10 Hz versus inverse gate voltage minus threshold voltage for different channel length TFTs.

5.2.2 The effect of channel length on the noise

It is easy to derive the expected dependence of noise on channel length. Consider a channel with length L that has a certain amount of resistance noise power S_R. The resistance of the channel is R and so the normalized noise power is S_R / R^2. If the channel length is now doubled to $2L$, the noise power of each section of length L will still be S_R but the noise of the sections are uncorrelated and so the total noise power is just $2S_R$. The resistance is now $2R$ so the

normalized noise is $2S_R/(2R)^2 = \frac{1}{2}S_R/R^2$. Thus, doubling the length of the channel halves the normalized noise power. In general, the normalized noise power will scale as $1/L$ as shown in Eq. 5.4; this relation is again an example of the general relation that normalized noise scales as the inverse of the volume of the sample.

The measured normalized noise magnitude at 10 Hz versus the inverse channel length for different gate voltages is shown in Fig. 5.4. The data set is the same as in the previous section (Fig. 5.3); it simply has been plotted in a new way. Again the experimental results are in qualitative agreement with the theory since the normalized noise increases as the channel length decreases. On a log-log plot, the slopes should be unity as predicted by Eq. 5.4. The slopes

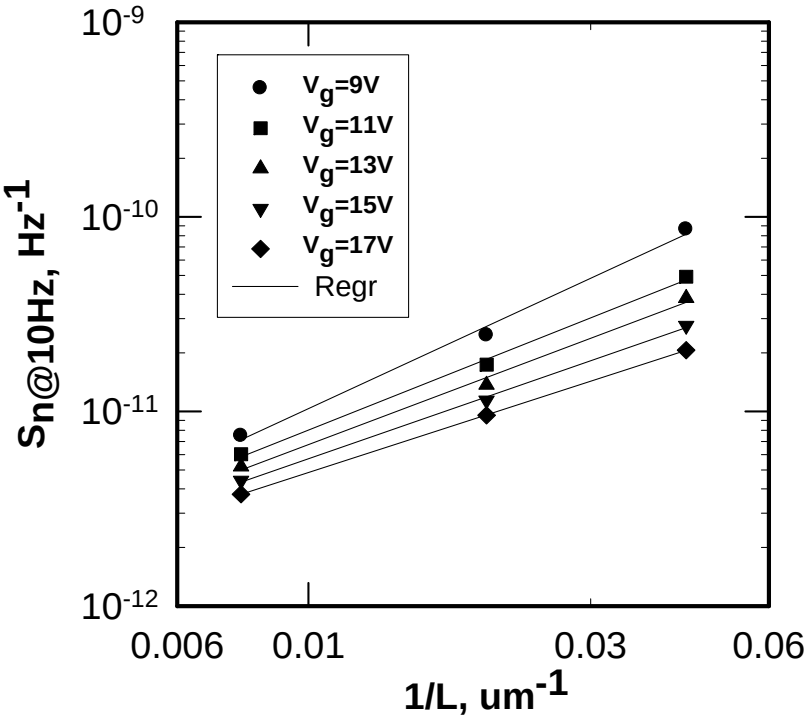


Figure 5.4 S_n at 10 Hz versus inverse channel length for different gate voltages.

obtained from a regression of the data are 1.4, 1.2, 1.1, 1.05 and 0.98 for the gate voltages of 9 V, 11 V, 13 V, 15 V and 17 V, respectively. Good agreement with theory is obtained for the higher gate voltages but the lowest gate voltage shows a stronger dependence of noise on channel length than expected.

5.3 The Effects of Drain-Source Voltage and Drain-Source Current on the Noise

In this section, I investigate the effects of drain-source voltage and current on the noise spectrum for the three TFTs. As shown in section 5.1, the normalized noise is almost independent of drain-source current. However, the fits to the data reveal a small residual dependence that can be explained by the device physics.

5.3.1 The effect of drain-source voltage

As described in the previous sections, each normalized noise spectrum was fit to the power law which yielded the noise power density at 10 Hz. Since a fit is a type of averaging that reduces scatter, the fitted parameters for the noise at 10 Hz provide a more precise determination of the noise dependence on drain-source voltage. Fig. 5.5a-c show the fitted normalized noise power at 10 Hz as a function of drain-source voltage for the gate voltages 9 V, 11 V, 13 V, 15 V, and 17 V. Each figure is for a different TFT. As shown in Fig. 5.5a-c, the normalized noise power weakly increases with drain-source voltage in all cases; the slopes of the power law fits are listed in Table 5.1.

Table 5.1 Power law exponents for S_n versus V_{ds}.

V_g / Aspect Ratio	9 V	11 V	13 V	15 V	17 V
0.23	0.36	0.29	0.25	0.2	0.15
0.5	0.09	0.16	0.18	0.16	0.15
1.3	0.28	0.19	0.16	0.12	0.11

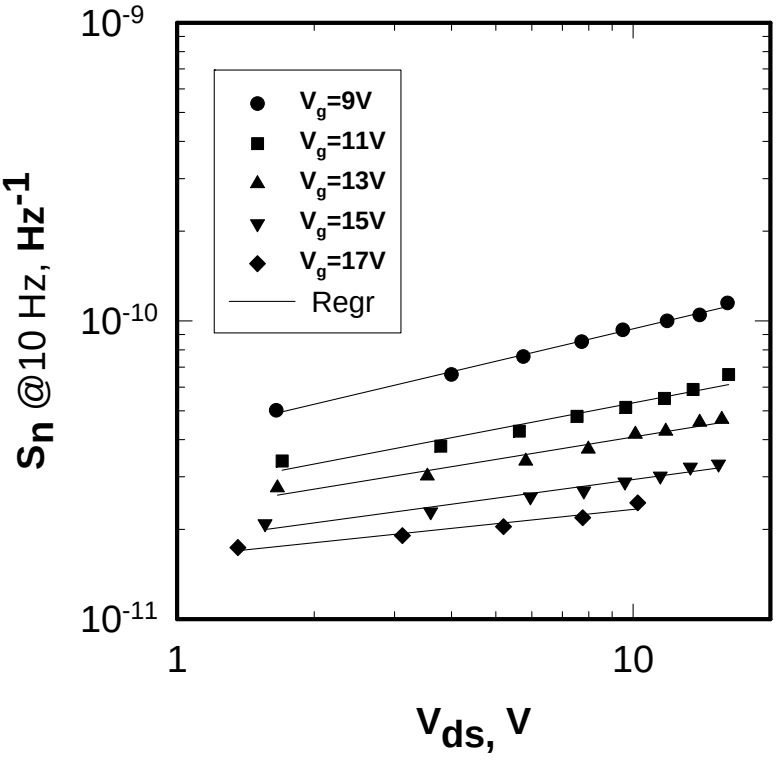


Figure 5.5a S_n at 10 Hz versus V_{ds} at different V_g for the 0.23 aspect ratio TFT.

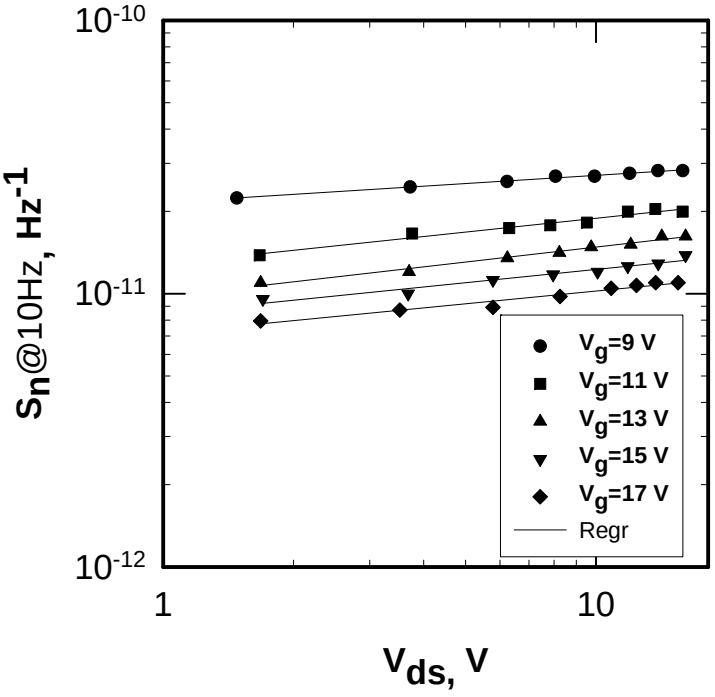


Figure 5.5b S_n at 10 Hz versus V_{ds} at different V_g for the 0.5 aspect ratio TFT.

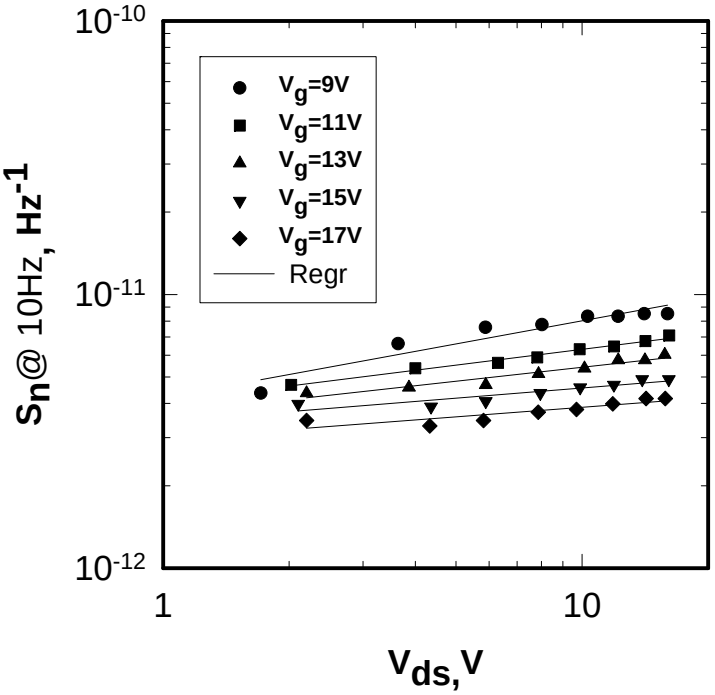


Figure 5.5c S_n at 10 Hz versus V_{ds} at different V_g for the 1.3 aspect ratio TFT.

The slight increase of the normalized noise power can be explained by channel length modulation or the Early effect [34][35]. The Early effect is a decrease in the length of the accumulation region of the channel as the drain-source voltage is increased. The decrease is caused by the pinch-off point shifting away from the drain. If the effective channel length is decreased by a shift of the pinch-off point then the normalized noise power will increase because the normalized noise power is inversely proportional to the channel length. The noise data can then be used to measure the relative decrease of channel length with drain-source voltage. From the data of Fig. 5.5b for the 0.5 aspect ratio TFT, I calculate the relative change of the channel length using change of the normalized noise power as V_{ds} is increased from 2 V to 16 V. For example, at the gate voltage of 9 V, the magnitude of the normalized noise power changes from 2.34×10^{-11} Hz^{-1} at $V_{ds}=2\,\text{V}$ to 2.89×10^{-11} Hz^{-1} at $V_{ds}=16\,\text{V}$. The relative change of the

normalized noise power is 1.24, and so the channel length decreased by a factor of 0.81; thus the effective channel length has been reduced from 50 μm to 40.5 μm. The results for different gate voltages are shown in Table 5.2.

The Early effect itself provides an independent way of calculating the reduction in effective channel length. At the start of the saturation region, the pinch-off point is at the drain and the effective channel length is equal to the drain -source separation. To a first approximation, the increase in current for larger drain-source voltages is due to the reduction in effective channel length as the pinch-off point moves away from the drain. The ratio of current at the start of the saturation to that at a higher V_{ds} times the drain-source separation (50 μm) is equal to the effective channel length, and this value can be compared with the value calculated from the noise measurements. The effective channel length calculated using the data from Fig. 4.2 for $V_{ds} = 16\,\mathrm{V}$ is shown in the last column of Table 5.2. Given the uncertainty in the calculations, especially choosing the point at which the pinch-off point first occurs, the agreement with the results from the noise measurements is acceptable.

Table 5.2 Effective channel length at $V_{ds} = 16\,\mathrm{V}$ for different gate voltages.

V_g (V)	S_n (10^{-11})(Hz^{-1})		Relative change of S_n	Ratio of channel length	Effective channel length(μm)	Channel length by Early effect(μm)
	V_{ds}=2V	V_{ds}=16V				
9	2. 34	2. 89	1. 24	0. 81	40.5	41
11	1. 49	2. 09	1. 40	0. 71	35.7	39
13	1. 14	1. 67	1. 46	0. 68	34.1	39
15	0. 97	1. 37	1. 41	0. 71	35.4	43
17	0.81	1.13	1.40	0.72	35.84	—

5.3.2. The effect of drain-source current

The normalized noise magnitude versus the drain-source current for different gate voltages is shown in Fig. 5.6a-c. The data is the same as in the previous section except that the plots are versus the current instead of the voltage. The graphs show that the normalized noise power increases with drain-source current. The increase is also explained by the Early effect. The decrease in the effective channel length is responsible for the increase of I_{ds} in the saturated region of the transfer curves; in the first approximation $I_{ds} \propto 1/L$. Since $S_n \propto 1/L$, we expect that $S_n \propto I_{ds}$ in the saturated region. The data of Fig. 5.6 are in qualitative agreement with this prediction as can be best seen for the 0.23 aspect ratio TFT (Fig. 5.6a).

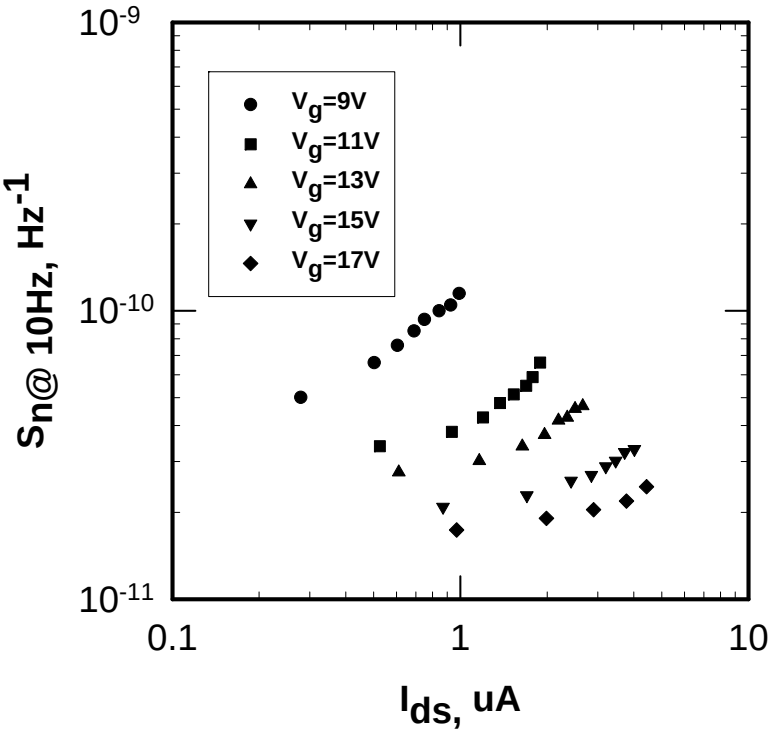


Figure 5.6a S_n at 10 Hz versus I_{ds} at different V_g for the 0.23 aspect ratio TFT.

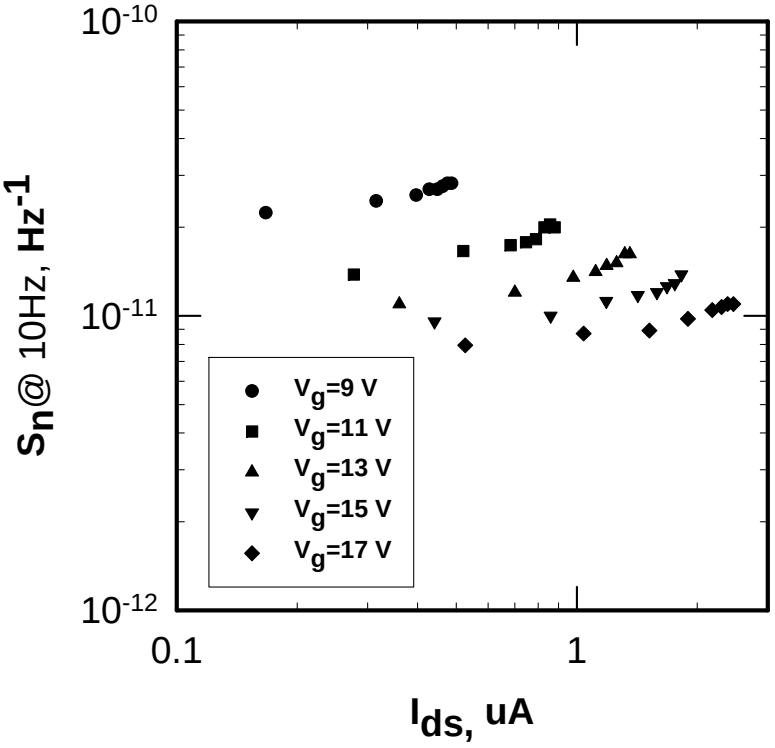


Figure 5.6b S_n at 10 Hz versus I_{ds} at different V_g for the 0.5 aspect ratio TFT.

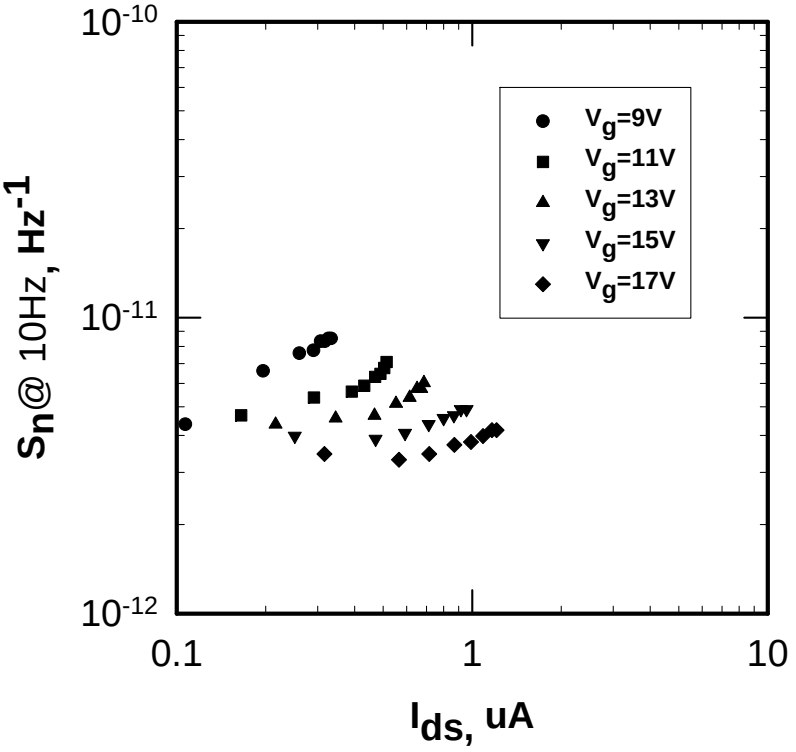


Figure 5.6c S_n at 10 Hz versus I_{ds} at different V_g for the 1.3 aspect ratio TFT.

5.4 The Effect of Gate-biasing Stress Time on the Noise

In this section, I investigate the measured relation between the normalized noise power density and the gate-biasing stress time. As mentioned in section 2.2.2.3, when a gate voltage is applied to a-Si:H TFTs, their transfer characteristics undergo a parallel shift. This shift is in effect a change in the threshold voltage; the amount of shift depends on the gate voltage biasing stress time. Annealing 180°*C* for 2 hours returns the TFTs to their initial characteristics. I measured the I-V characteristics and the noise spectra for various gate-biasing stress times.

5.4.1 The Effect of Positive Gate-biasing Stress

The changes in the I-V characteristics with increasing time of positive gate-biasing stress for the 0.23 aspect ratio TFT are illustrated in Fig. 5.7. The density of defect states increases, as the longer a gate voltage is applied to the a-Si:H TFT. As a result, more of the carriers in the channel go to fill up the new states, and thus the number of mobile carriers is reduced and so the drain-source current is decreased. Since the transfer characteristics obey $I_{ds} \propto (V_g - V_T)^2$, the threshold voltage is the intercept of a plot of $I_{ds}^{1/2}$ versus V_g; the shift in the threshold voltage is obvious in such a plot. Fig. 5.8 shows the threshold voltage shift for positive gate-biasing. The threshold voltage increases from 2.5 V to 4 V after 95.5 hours of biasing stress with a gate voltage of 15 V. Most of the shift occurred after only 24 hours of stress.

After each step in the stress schedule, the normalized noise power was measured. There is no measurable change in the spectra due to the gate biasing stress. In order to increase the sensitivity to any change, the noise power is numerically integrated over a specific frequency band. The integrated normalized noise power *K* is

$$K = \int_{f1}^{f2} S_n df \qquad (5.12)$$

where f_1 and f_2 are taken as 2 Hz and 27 Hz, respectively. As shown in Fig 5.9, the integrated noise power is almost unchanged with up to 95 hours of gate biasing stress; thus, the gate-biasing stress time has no effect on the normalized noise power.

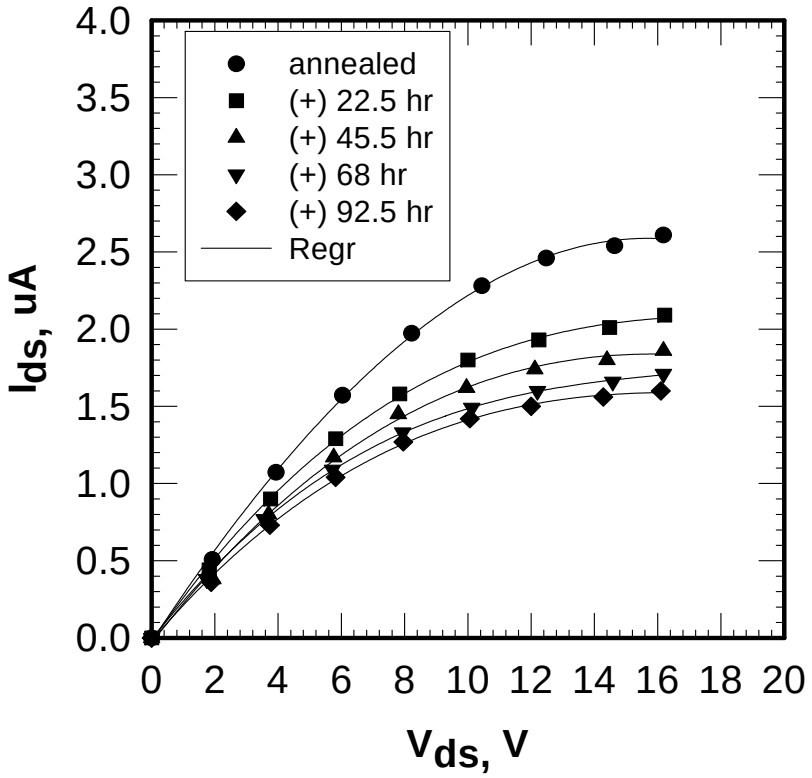


Figure 5.7 I-V characteristics after positive gate-biasing stress for the 0.23 aspect ratio TFT.

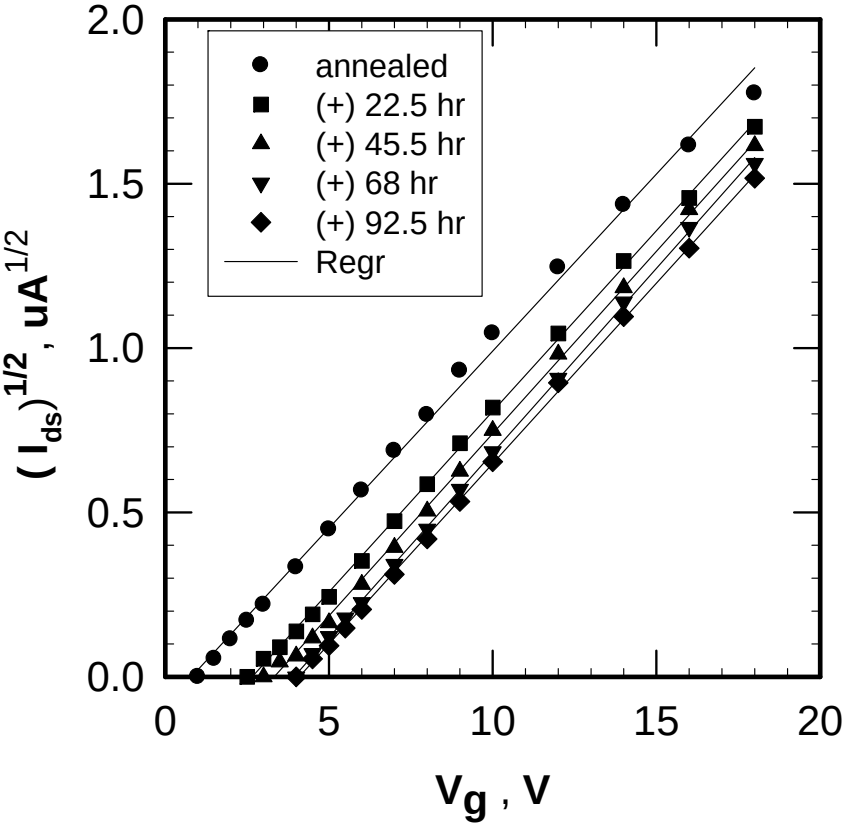


Figure 5.8 Threshold voltage shift after positive gate-biasing times for the 0.23 aspect ratio TFT.

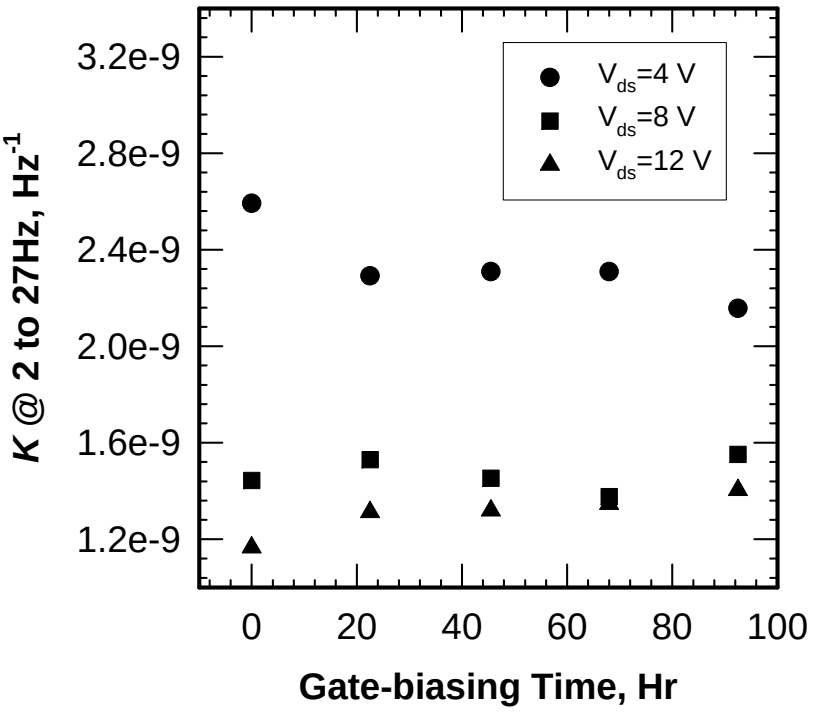


Figure 5.9 Integrated noise power versus positive gate-biasing stress for the 0.23 aspect ratio TFT.

5.4.2 The Effect of Continuous Negative and Positive Gate-biasing Stress Time

With the 0.5 aspect ratio TFT, I measured the I-V characteristic, the threshold voltage and the normalized noise power after applying a negative gate voltage of -15 V for 62.5 hours and then measured them again after a applying positive gate voltage of 15 V for 24 hours. A gate voltage of 15 V was used to measure the I-V characteristics, and a drain-source voltage of 13 V was used to determine the threshold voltage. The noise spectra were measured using drain-source voltages of 4 V, 8 V, and 12V and a gate voltage of 15 V. As shown in Fig. 5.10, the drain-

source current is reduced by the negative gate voltage stress and the positive stress caused a small further reduction. The threshold voltage shift for negative and positive gate-biasing stress is shown in Fig. 5.11. Although the slope after the negative gate biasing stress time changes, a clear shift in the threshold voltage occurs in the same direction as after the positive stress. In contrast, Tsukada [3] observed a shift to the right for positive gate voltages and to the left for negative gate voltages. As discussed in section 2.2.2.3, the shifts I observe indicates that the gate voltage stress is creating extra deep defect states whereas the shifts Tsukada observed imply charge trapping in the insulator.

Fig. 5.12 shows the integrated noise power K versus the gate-bias stress time for applying continuous negative and positive gate voltage. Again K is independent of stress time for either positive or negative gate-biasing; thus, the normalized noise power has no connection to the changes that take place with gate-biasing stress.

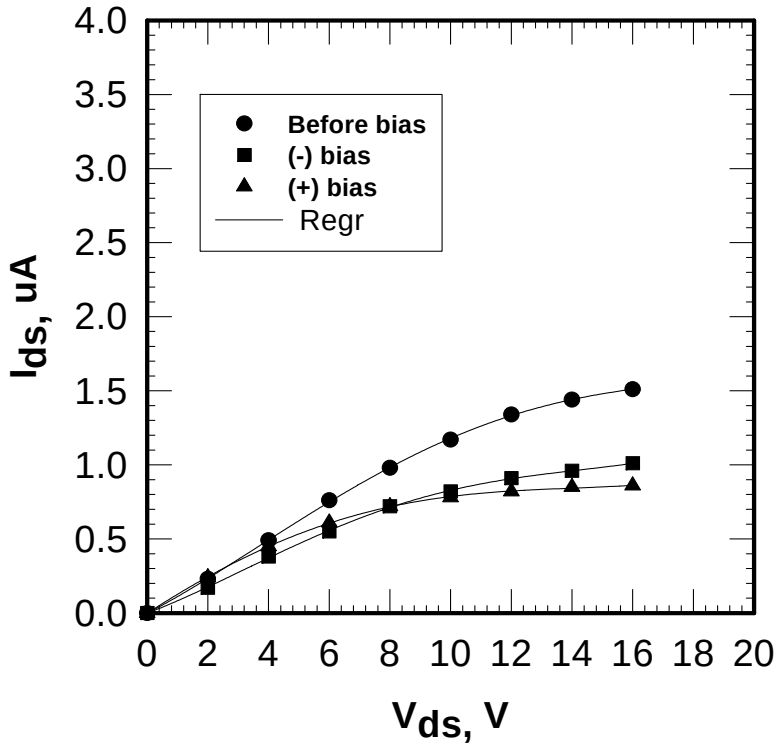


Figure 5.10 I-V characteristics after negative and positive gate-biasing time for the 0.5 aspect ratio TFT.

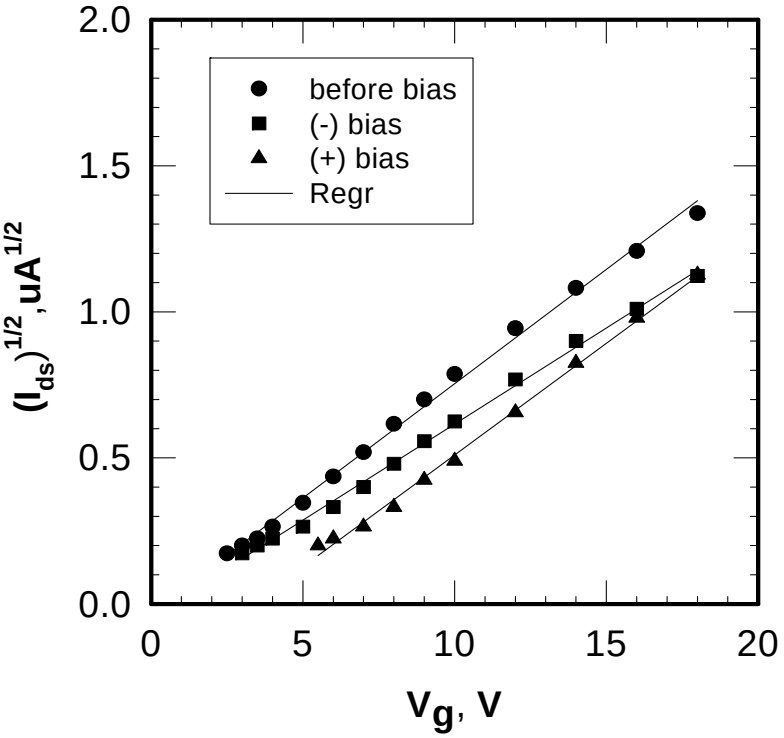


Figure 5.11 Threshold voltage shift after positive and negative gate-biasing time for the 0.5 aspect ratio TFT.

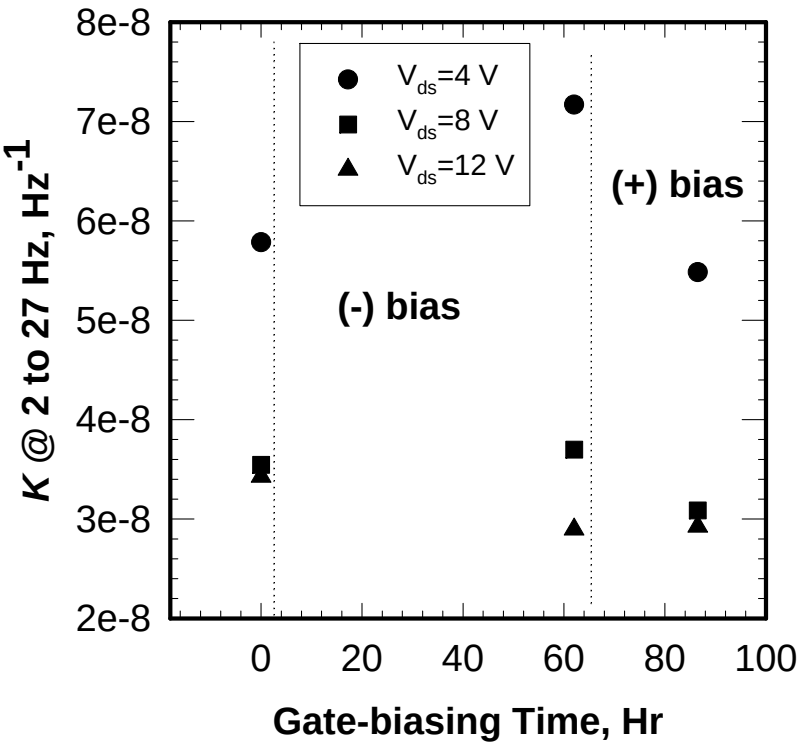


Figure 5.12 The integrated noise power versus the gate-bias stress time for the 0.5 aspect ratio TFT.

5.5 Hooge's Parameter

Section 3.1.3 introduced Hooge's emperical formula relating the normalized noise to the number of carriers in the device *N*. The parameter α_H in Eq. 3.5 is often used as a measure of the amount of noise in a device or material. With the a-Si:H TFTs, a difficulty arises in determining *N* since many of the carriers in the channel are trapped. Should *N* include all the carriers making up the accumulation layer's charge or just the ones that are mobile? I estimate the number of trapped carriers and the number of free carriers as a function of gate voltage and channel thickness. These values are used to calculate Hooge's parameter in several ways.

5.5.1 The number of trapped carriers

The number of the carriers in the accumulation layer that are trapped depends on the density of states in a-Si:H. The calculations in this section use the simplified model of the density of states shown in Fig. 5.13. It consists of a Gaussian shaped peak of defect states centered around 0.8 eV below the conduction band mobility edge E_C and an exponential band tail.

$$g(E) = \frac{g_{\max}}{\sqrt{\pi} E_w} e^{-\left(\frac{E-E_d}{E_w}\right)^2} + g_C e^{\frac{E}{KT_0}} \tag{5.13}$$

where $g_C = 10^{21}\,\text{cm}^{-3}$, $kT_0 = 0.0284\,\text{eV}$, $g_{\max} = 10^{16}\,\text{cm}^{-3}$, $E_d = -0.8\,\text{eV}$, and $E_w = 0.2\,\text{eV}$; all energies are measured with respect to E_C which is taken to be zero. The values are typical for good quality a-Si:H.

When a gate voltage is applied to the sample TFT, some of the carriers in the accumulation layer are trapped in the localized states, and the Fermi level shifts from E_F to E_F'. The density of trapped carriers can be calculated from the density of states and the change in the Fermi level by

$$\Delta n_{\text{trap}} = \int^{E_C} [g(E) f(E_F') - g(E) f(E_F)] dE \tag{5.14}$$

where f is the Fermi function. The change in the number of free carriers is determined by the Fermi level positions

$$\Delta n_{\text{free}} = N_c [e^{E_F'/kT} - e^{E_F/kT}] \tag{5.15}$$

where $N_C = kTg_C$. Finally the total density of carriers in the accumulation layer is

$$\Delta n_{\text{total}} = \Delta n_{\text{trap}} + \Delta n_{\text{freel}} \tag{5.16}$$

The density of free and trapped carriers are calculated as a function of E_F' and shown in Table 5.3; the initial position of the Fermi level was taken equal to the center of the defect band E_d.

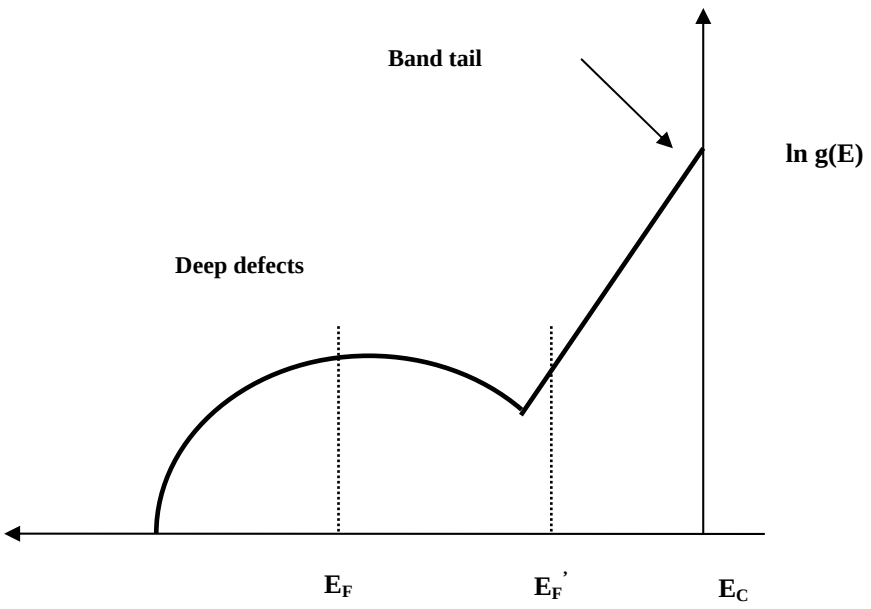


Figure 5.13 The density of state in a-Si:H TFTs.

The total density of carriers for a given gate voltage can be calculated from the gate capacitance.

$$\Delta n_{total} = \frac{Q}{qV} = \frac{C_g V_g}{qV} = \frac{C_{ins} WLV_g}{qWLd} = \frac{C_{ins} V_g}{qd} \tag{5.17}$$

where d is the channel thickness, the gate capacitance is $C_g = C_{ins} WL$, and the insulator distributed capacitance is $C_{ins} = \varepsilon_{ins}\varepsilon_0 / t_{ins} = 17.7 \times 10^{-5}\ \mathrm{F/m^2}$, where the relative permittivity of the insulator ε_{ins} is 6~7, and the thickness of the insulator t_{ins} is 300 nm. Table 5.4 gives Δn_{total} for V_g from 1 V to 17 V using 100 μm for the channel width W, 23 μm for the channel length L, and 2 nm for the channel thickness d.

Table 5.3 Densities of trapped, free, and total carriers for various Fermi levels

E_c-E_f' (eV)	Δn_{trap} (E18) (cm^{-3})	Δn_{free} (E18) (cm^{-3})	Δn_{total} (E19) (cm^{-3})	E_c-E_f' (eV)	Δn_{trap} (E18) (cm^{-3})	Δn_{free} (E18) (cm^{-3})	Δn_{total} (E19) (cm^{-3})
0.061	**7.07**	**2.44**	**0.9516**	0.094	3.09	0.68	0.3772
0.062	6.91	2.35	0.9262	0.095	3.01	0.66	0.3664
0.063	6.75	2.26	0.9014	0.096	2.93	0.63	0.3559
0.064	6.60	2.17	0.8772	0.097	2.85	0.61	0.3457
0.065	6.44	2.09	0.8537	0.098	2.77	0.58	0.3358
0.066	6.29	2.01	0.8307	0.099	2.70	0.56	0.3261
0.067	6.15	1.94	0.8082	0.1	2.63	0.54	0.3167
0.068	6.00	1.86	0.7863	0.101	2.56	0.52	0.3076
0.069	5.86	1.79	0.7650	0.102	2.49	0.50	0.2987
0.07	5.72	1.72	0.7442	0.103	2.42	0.48	0.2900
0.071	5.58	1.66	0.7239	**0.104**	**2.35**	**0.46**	**0.2816**
0.072	5.45	1.60	0.7042	0.105	2.29	0.45	0.2734
0.073	5.31	1.54	0.6849	0.106	2.23	0.43	0.2654
0.074	5.18	1.48	0.6661	0.107	2.16	0.41	0.2577
0.075	5.06	1.42	0.6478	0.108	2.11	0.40	0.2502
0.076	4.93	1.37	0.6299	0.109	2.05	0.38	0.2429
0.077	**4.81**	**1.32**	**0.6125**	0.11	1.99	0.37	0.2358
0.078	4.69	1.27	0.5956	0.111	1.94	0.35	0.2288
0.079	4.57	1.22	0.5791	0.112	1.88	0.34	0.2221
0.08	4.46	1.17	0.5630	0.113	1.83	0.33	0.2156
0.081	4.35	1.13	0.5473	0.114	1.78	0.31	0.2092
0.082	4.24	1.08	0.5320	0.115	1.73	0.30	0.2031
0.083	4.13	1.04	0.5172	0.116	1.68	0.29	0.1971
0.084	**4.02**	**1.00**	**0.5027**	0.117	1.63	0.28	0.1912
0.085	3.92	0.97	0.4886	0.118	1.59	0.27	0.1856
0.086	3.82	0.93	0.4748	0.119	1.54	0.26	0.1801
0.087	3.72	0.89	0.4614	**0.12**	**1.50**	**0.25**	**0.1747**
0.088	3.62	0.86	0.4484	0.121	1.46	0.24	0.1696
0.089	3.53	0.83	0.4357	0.122	1.41	0.23	0.1645
0.09	3.44	0.80	0.4234	0.123	1.37	0.22	0.1596
0.091	3.35	0.77	0.4114	0.124	1.34	0.21	0.1549

Table 5.4 Density of total carriers for different gate voltages using $d = 2\,\text{nm}$.

V_g (V)	Density of carriers (cm^{-3})
1	5.5E+17
3	1.7E+18
5	2.8E+18
7	3.9E+18
9	5.0E+18
11	6. 1E+18
13	7. 2E+18
15	8. 3E+18
17	9. 4E+18

For each of the values of Δn_{total} in Table 5.4, Table 5.3 is used as a lookup table to determine the value of E_F' that corresponds to that value of Δn_{total}. The result is shown in Table 5.5 which gives for each gate voltage the density of free and trapped carriers and the percentage of free carriers. Notice that for all gate voltages, most of the carriers are trapped as shown in Fig. 5.14.

Table 5.5 Densities of trapped, free, and total carriers for various gate voltages.

V_g(V)	E_c-E_f(eV)	Δn_{trap} (cm^{-3})	Δn_{free}(cm^{-3})	Δn_{total}(cm^{-3})	Δn_{free} (%)
1	0. 158	4. 9 E+17	0. 6 E+17	5. 4E+17	10. 53
3	0. 12	1. 5 E+18	0. 2 E+18	1. 7 E+18	14. 27
5	0. 104	2. 3 E+18	0. 4 E+18	2. 8 E+18	16. 44
7	0. 093	3. 1 E+18	0. 7 E+18	3. 9 E+18	18. 24
9	0. 084	4. 0 E+18	1. 0 E+18	5. 0 E+18	19. 96
11	0. 077	4. 8 E+18	1. 3 E+18	6. 1 E+18	21. 47
13	0. 071	5. 5 E+18	1. 6 E+18	7. 2 E+18	22. 91
15	0. 066	6. 2 E+18	2. 0 E+18	8. 3 E+18	24. 23
17	0. 061	7. 0 E+18	2. 4 E+18	9. 5 E+18	25. 66

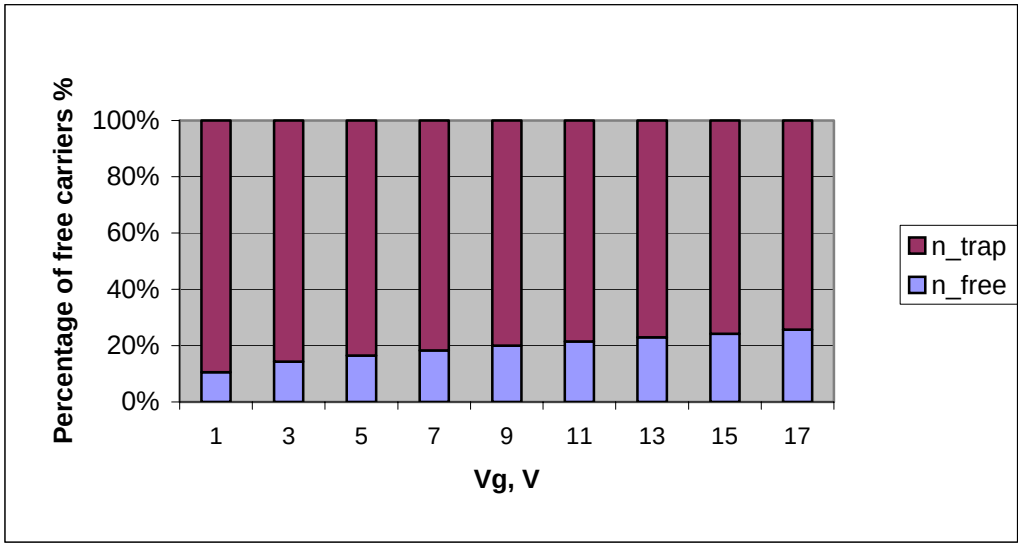


Figure 5.14 Relative numbers of free and trapped carriers at various gate voltages.

The thickness of the channel is not actually known, but Goodman [36] stated that 90 percent of the current flows within a 1–5 nm thick layer adjacent to the interface. I used an arbitrary value in the middle of this range. However, to judge how sensitive the results are to the channel thickness, I also calculated the percentage of free carriers for channel thicknesses of 1 nm and 5 nm. The results are compared to those for a 2 nm channel thickness as shown in Fig.5.15. Over the gate voltage range of 2 V to 10 V, the free carrier percentages are within 10 % for the lower gate voltages and up to 28 % for the highest gate voltage for the three channel thicknesses with the thinner channels having a higher percentage of free carriers.

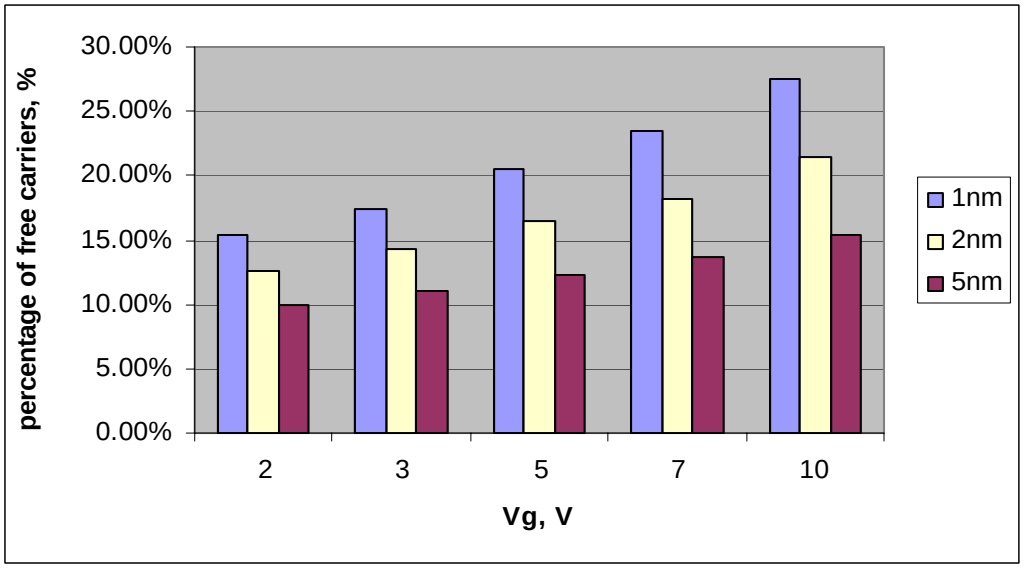


Figure 5.15 Percentage of free carriers for various gate voltages.

5.5.2 Hooge's Parameter in a-Si:H TFTs

Hooge's parameter α_H is useful to characterize the magnitude of low frequency noise in materials and devices. Hooge originally claimed α_H is a constant for all materials, but later measurements showed that the value is different for different semiconductor structures and devices, ranging from 2×10^{-3} for long resistors or pn junction diodes to 1×10^{-5} for GaN HFET's or 1×10^{-8} for short channel GaAs FET's and BJT's [37]. In the a-Si:H TFTs, most channel carriers are trapped in localized states, so it is not clear what value should be used for N in Hooge's empirical relation Eq. 5.3, N_{total} or N_{free}. I calculate α_H both ways using the values for the free and total charge densities found in the previous section; Fig. 5.16 shows α_H versus gate voltage. Hooge's parameter is in the range 1-2$\times10^{-3}$ using N_{total} and 2-4$\times10^{-4}$ using N_{free}. Either set of values indicates that the a-Si:H TFTs are relatively noisy compared to other FETs.

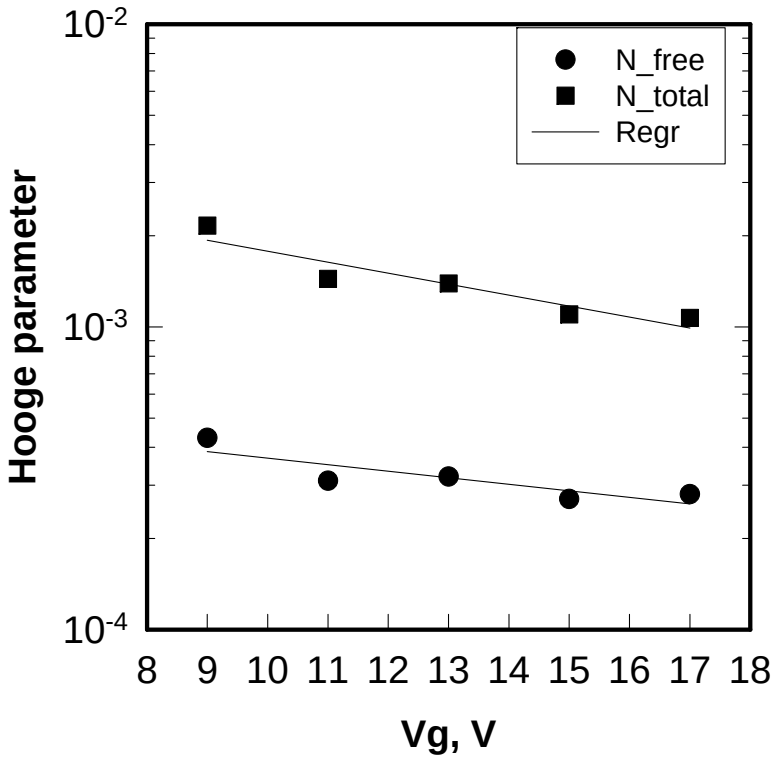


Figure 5.16 Hooge's parameter versus gate voltage.

5.6 The Signal to Noise Ratio (SNR)

The signal-to-noise ratio in an X-ray imaging detector is an important factor determining the performance of the detector. As mentioned at the introductory material, X-ray imaging detectors are divided into two types: indirect X-ray detectors and direct X-ray detectors. The indirect X-ray detectors include a scintillator layer, an amorphous silicon photodiode layer and amorphous silicon TFT layer. In this section, I calculate the signal-to-noise ratio (S/N) component produced by the noise of an a-Si TFT connected to a photodiode [10] [38] [39] [40]. The photodiode at each pixel converts incident light to current, and the TFT is used to gate the

current to a charge sensitive, integrating amplifier. Due to the channel noise of the TFT, the current will fluctuate leading to a variance in the amount of charge collected. I first derive the mathematical relation between the current fluctuations and the variance in the charge and then use the experimental noise measurements to calculate the SNR for different channel lengths and different gate voltages.

5.6.1 Theory

The TFT is turned on for a time *T*. The charge *Q* collected is the integral of the current signal that has a stationary, random component $x(t)$; $\bar{x} = 0$. *Q* can be written as an average value plus a fluctuating value $Q = \overline{Q} + q(t)$ where

$$q(t) = \int_0^T x(t)dt \tag{5.18}$$

We need to relate the variance in *q* to the noise spectrum of $x(t)$.

$$\begin{aligned} \mathrm{Var}(q) &= < q^2 > \\ &= < \int_0^T x(t_1)dt_1 \int_0^T x(t_2)dt_2 > \\ &= < \int_0^T \int_0^T x(t_1)x(t_2)dt_1dt_2 > \\ &= \int_0^T \int_0^T < x(t_1)x(t_2) > dt_1dt_2 \end{aligned} \tag{5.19}$$

where the brackets (<>) means a time average. But $< x(t_1)x(t_2) >$ is the autocorrelation function $R(t_1,t_2)$ for the signal $x(t)$; it is also the auto-covariance function $C(t_1,t_2)$, since $R(t_1,t_2) = C(t_1,t_2)$ if $\bar{x} = 0$. Therefore, the variance in *q* is related to the autocorrelation of the fluctuating part of the signal

$$\mathrm{Var}(q) = \int_0^T \int_0^T R(t_1,t_2)dt_1dt_2 \tag{5.20}$$

For a WSS (Wide Sense Stationary) process, $R(t_1,t_2)=R(\tau)$, where $\tau=t_1-t_2$, and Eq. 5.20 becomes after some manipulation [41]

$$\mathrm{Var}(q)=2\int_0^T (T-\tau)R(\tau)d\tau \tag{5.21}$$

The noise spectrum of $x(t)$, $S(\omega)$, and the autocorrelation function, $R(\tau)$, are related by the Fourier transform

$$S(\omega)=\int_{-\infty}^{\infty} R(\tau)e^{-j\omega\tau}d\tau \quad \text{and} \quad R(\tau)=\frac{1}{2\pi}\int_{-\infty}^{\infty} S(\omega)e^{j\omega\tau}d\omega \tag{5.22}$$

Since $R(\tau)=R^*(-\tau)$, $S(\omega)$ is real, and since $x(t)$ is real, both R and S are real and even functions. Thus if we know $S(\omega)$, we can calculate $R(\tau)$ and then $Var(q)$ from Eq. 5.21.

First let $S(\omega)$ be pure $1/f$ noise

$$S(\omega)=\frac{S_0}{|\omega|} \tag{5.23}$$

$R(\tau)$ is calculated from Eq. 5.22

$$R(\tau)=\frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{S_0}{|\omega|}e^{j\omega\tau}d\omega \tag{5.24}$$

Notice that the lower half of the integral (from -∞ to 0) can be rewritten (using the variable substitution $\omega'=-\omega$)

$$\int_{-\infty}^{0}\frac{S_o}{|\omega|}e^{j\omega\tau}d\omega=-\int_{\infty}^{0}\frac{S_0}{|\omega'|}e^{-j\omega'\tau}d\omega'=\left(\int_0^{\infty}\frac{S_0}{|\omega'|}e^{j\omega'\tau}d\omega'\right)^* \tag{5.25}$$

Thus the lower half of the integral is simply the complex conjugate of the upper half of the integral. Therefore, Eq. 5.24 becomes

$$\begin{aligned} R(\tau)&=\frac{1}{2\pi}2\,\mathrm{Re}\int_0^{\infty}\frac{S_0}{|\omega|}e^{j\omega\tau}d\omega \\ &=\frac{1}{\pi}\int_0^{\infty}\frac{S_0}{|\omega|}\cos(\omega\tau)d\omega \end{aligned} \tag{5.26}$$

Unfortunately the integral in Eq. 5.26 diverges. To prevent this divergence, we need to impose a low frequency cut-off of the noise spectrum. So instead of the pure 1/*f* spectrum of Eq. 5.23, let

$$S(\omega) = \frac{S_0}{(\omega_x{}^2 + \omega^2)^{1/2}} \tag{5.27}$$

for $\omega << \omega_x$, $S(\omega) = S_0 / \omega_x$ a constant, and for $\omega >> \omega_x$, $S(\omega) = S_0 / \omega$.

Equation 5.26 now becomes

$$R(\tau) = \frac{1}{\pi} \int_0^\infty \frac{S_0}{(\omega_x{}^2 + \omega^2)^{\frac{1}{2}}} \cos(\omega\tau) d\omega \tag{5.28}$$

The integral evaluates to a Bessel function of the 2nd kind, since

$$\int_0^\infty \frac{\cos(ax)}{(\beta^2 + x^2)^{1/2}} dx = K_0(a\beta) \tag{5.29}$$

The autocorrelation function is

$$R(\tau) = \frac{S_0}{\pi} K_0(\omega_x \tau) \tag{5.30}$$

and finally, from Eq. 5.21

$$\mathrm{Var}(q) = 2 \int_o^T (T - \tau) \frac{S_0}{\pi} K_0(\omega_x \tau) d\tau \tag{5.31}$$

If $T << 1/\omega_x$, the Bessel function can be approximated by the expansion

$$K_0(x) \sim -\gamma - \ln \frac{x}{2} + ... \text{ for small argument} \tag{5.32}$$

and the integral can be evaluated in closed form

$$
\begin{aligned}
\mathrm{Var}(q) &= 2\int_o^T (T-\tau)\frac{S_0}{\pi}[-\gamma-\ln\frac{\omega_x\tau}{2}]d\tau \\
&= \frac{2S_0}{\pi}\int_0^T -\gamma T+\gamma\tau-T\ln\frac{\omega_x\tau}{2}+\tau\ln\frac{\omega_x\tau}{2}\,d\tau \\
&= \frac{2S_0}{\pi}[-\gamma T^2+\frac{\gamma}{2}T^2-T\tau(\ln\frac{\omega_x\tau}{2}-1)\Big|_0^T+\tau^2(\frac{1}{2}\ln\frac{\omega_x\tau}{2}-\frac{1}{4})\Big|_0^T] \qquad (5.33)\\
&= \frac{2S_0}{\pi}[-\frac{\gamma}{2}T^2-T^2(\ln\frac{\omega_x T}{2}-1)+T^2(\frac{1}{2}\ln\frac{\omega_x T}{2}-\frac{1}{4})] \\
&= \frac{2S_0}{\pi}T^2[\frac{3}{4}-\frac{\gamma}{2}-\frac{1}{2}\ln\frac{\omega_x T}{2}]
\end{aligned}
$$

where $\gamma = 0.577$ is the Euler-Mascheroni constant.

The signal-to-noise ratio for a pixel is expressed as

$$
\begin{aligned}
SNR &= \frac{\overline{Q}}{\delta Q} = \frac{I_0 T}{\sqrt{\mathrm{Var}(q)}} \\
&= \frac{I_0 T}{T\sqrt{\frac{2S_0}{\pi}[\frac{3}{4}-\frac{\gamma}{2}-\frac{1}{2}\ln\frac{\omega_x T}{2}]}} \qquad (5.34)\\
&= \frac{I_0}{\sqrt{\frac{2S_0}{\pi}[\frac{3}{4}-\frac{\gamma}{2}-\frac{1}{2}\ln\frac{\omega_x T}{2}]}}
\end{aligned}
$$

where I_0 is the average current, $\overline{Q} = I_0 T$. Notice that the SNR is only weakly dependent on the integration time *T*.

5.6.2 The experimental result and discussion

In this section, I calculate the SNR versus drain-source current using Eq. 5.34 for different channel lengths and gate voltages. The cut-off frequency is unknown and will be arbitrarily set to 0.159 Hz; the integration time *T* is taken to be 10 ms. If ω_x is lower than the value assumed then the SNRs will correspondingly be lowered. The value of S_0 comes from the noise measurements. Figure 5.17 shows the calculated SNR which are in the range of 45 to 47dB. Higher SNR is achieved for higher gate voltage. Figure 5.18 shows the SNR for TFTs with the

three channel lengths at a gate voltage of 13 V. Higher SNR is achieved using a TFT with a longer channel. This result comes from the relationship between noise power and channel lengths as mentioned in the section 5.2.

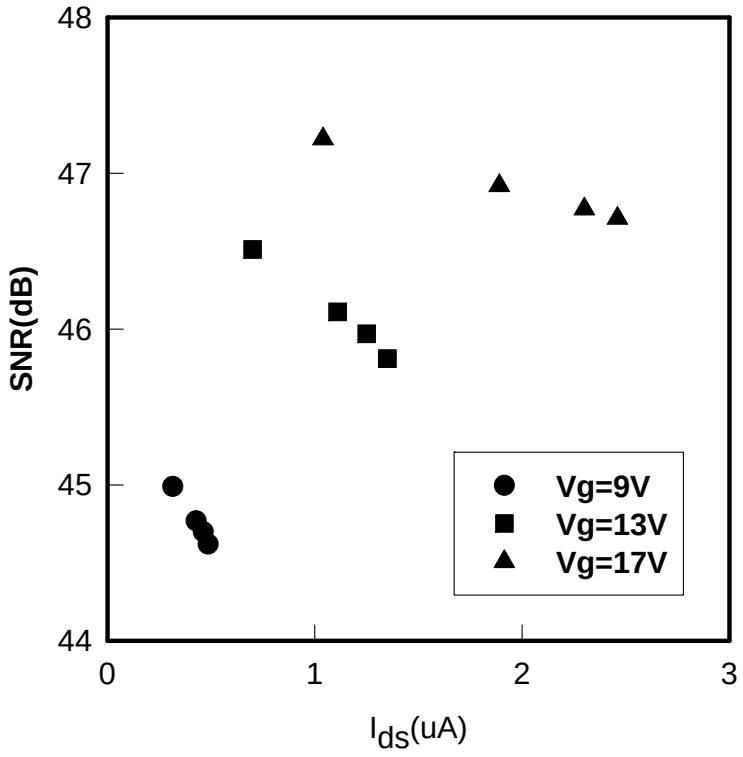


Figure 5.17 SNR versus gate voltage at the 0.5 aspect ratio TFT.

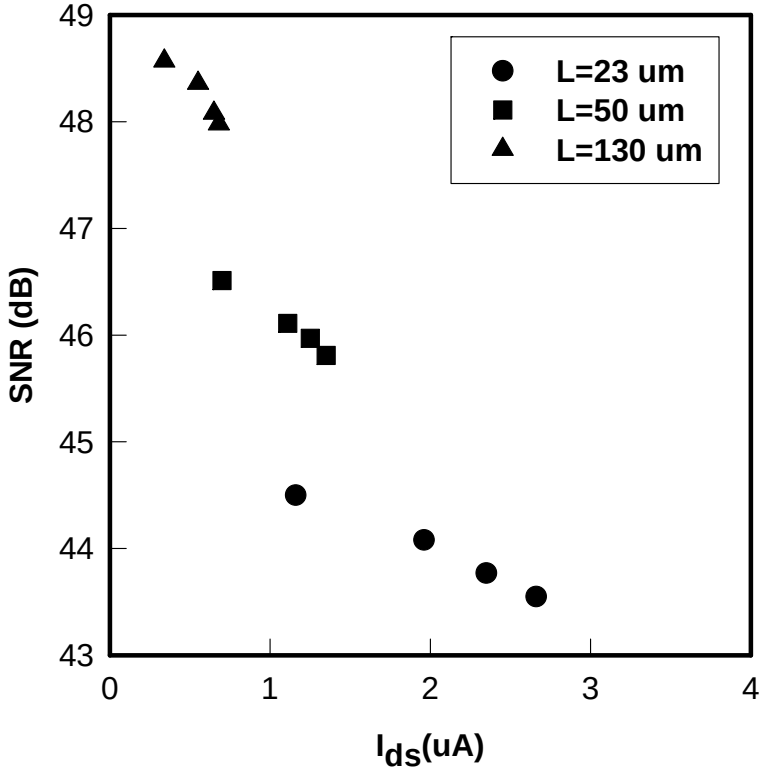


Figure 5.18 SNR versus channel length.

6. SUMMARY AND CONCLUSIONS

I have presented a study of the low frequency noise in hydrogenated amorphous silicon, thin-film transistors. Measurements of the noise spectrum show that the noise is nearly pure $1/f$ noise in the frequency range of 1 to 1000 Hz. The magnitude of the noise is inversely proportional to gate voltage which can be understood as the effect of the number of carriers in the accumulation layer. The magnitude is also inversely proportional to the channel length which is an effect of the active volume; a larger volume leads to lower normalized noise. The drain-source voltage was found to have a minor effect on the noise which was also attributed to a volume effect due to a change in the pinch-off point. In addition, changes in the transfer curves due to gate-biasing stress have no effect on the noise. The Hooge's parameter, which is a measure of how noisy the device is, was in the range $2\text{-}4\times10^{-4}$ when only the free carriers are used in Hooge's formula or $1\text{-}2\times10^{-3}$ if the total number of carriers is used. Finally, I calculated the signal-to-noise ratio in an example application of the TFTs, namely an indirect X-ray detector. The contribution of the TFT noise amounted to an SNR of about 45-47dB. Higher SNR is achieved for higher gate voltages and longer channel lengths.

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